

# **TB-7Z-IAE Hardware User Manual**

Rev.1.04

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## Revision History:

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Rev.1.04	2015/10/06	Update for TB-7Z-IAE Rev3 Added information : 3. Feature Updated information : 7. Main Specification Added information : 8. Board Specification Added information : 10.2. Power supply structure Updated information : 10.3. Clock structure Added information: 10.4. Board status LED Added information: 10.5.6. PS_POR_B_MR, PS_SRST Added information: 10.6. Fixing screw hole Added information: 10.8. microSD card socket (CN902) Added information: 10.12. QSPI Flash Added information: 10.13. F-RAM Added information: 10.14. RTC	Kiguchi

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## Introduction

Thank you for purchasing the “TB-7Z-IAE” board. This user manual contains important information when it is used in development and functional evaluation of the TB-7Z-IAE board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual and then always keep it handy.

If the TB-7Z-IAE board is incorporated in other products, refer to the respective delivery specification which contains definition of board specification, use conditions, guarantee conditions and others.




## SAFETY PRECAUTIONS

Be sure to observe these precautions




Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

 <b>Danger</b>	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
 <b>Warning</b>	Indicates the possibility of serious injury or death if the product is handled incorrectly.
 <b>Caution</b>	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.  
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.



## Warning



### **In the event of a failure, disconnect the power supply.**

If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.



### **If an unpleasant smell or smoking occurs, disconnect the power supply.**

If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.



### **Do not disassemble, repair or modify the product.**

Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.



### **Do not touch a cooling fan.**

As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.



### **Do not place the product on unstable locations.**

Otherwise, it may drop or fall, resulting in injury to persons or failure.



### **If the product is dropped or damaged, do not use it as is.**

Otherwise, a fire or electric shock may occur.



### **Do not touch the product with a metallic object.**

Otherwise, a fire or electric shock may occur.



### **Do not place the product in dusty or humid locations or where water may splash.**

Otherwise, a fire or electric shock may occur.



### **Do not get the product wet or touch it with a wet hand.**

Otherwise, the product may break down or it may cause a fire, smoking or electric shock.



### **Do not touch a connector on the product (gold-plated portion).**

Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

**Caution****Do not use or place the product in the following locations.**

- Humid and dusty locations
- Airless locations such as closet or bookshelf
- Locations which receive oily smoke or steam
- Locations exposed to direct sunlight
- Locations close to heating equipment
- Closed inside of a car where the temperature becomes high
- Staticky locations
- Locations close to water or chemicals

Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.

**Do not place heavy things on the product.**

Otherwise, the product may be damaged.

## Disclaimer

This product is an evaluation board intended for evaluation of Xilinx's **Zynq™-7000 All Programmable SoC**. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

- (1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions.
- (2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
- (3) Use of this product against the instructions given in this manual.
- (4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

- (1) Erasure or corruption of data arising from use of this product.
- (2) Any consequences or other abnormalities arising from use of this product, or
- (3) Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.



## 1. Related documents:

All documents relating to this board can be downloaded from our website.

### Board Fixture:

- Jumper short pin x 4

## 2. Overview

This product is an embedded module **TB-7Z-IAE** with Xilinx's **Zynq®-7000 All Programmable SoC** device (hereafter referred to as **Zynq**) for use of industrial networking products.

## 3. Feature

- ❑ High performance embedded module consolidating Zynq and peripheral devices
- ❑ Can support a wide variety of industrial network protocols by combining 2ch Gigabit Ethernet with Zynq Programmable Logic (PL)
- ❑ High performance 32bit 1,066Mbps DDR3 SDRAM operating up to 512MByte
- ❑ 16MByte Serial NOR Flash, Nonvolatile F-RAM™, microSD™ card socket for non-volatile data storage (microSD memory card is not included)
- ❑ B2B connector with 70 configurable user IOs and USB 2.0
- ❑ +5V single input power source having power supply sequence control function
- ❑ Environmental tests
  - IEC 61000-4-2:2008
  - IEC 61000-4-3:2006+A1:2007+A2:2010
  - IEC 61000-4-4:2012
  - IEC 61000-4-5:2005
  - IEC 61000-4-6:2008
  - IEC 61000-4-8:2009
  - IEC 61000-4-11:2004
  - EN 55022:2010 (Class A)
  - EN 60950-1:2006 + A2:2013 Class III
    - ✧ Power Input Test
    - ✧ Temperature Rise Measurement
    - ✧ Impulse Test
  - 1000Base-T Compliance Test
  - 100Base-TX Compliance Test
- ❑ RoHS Directive

## 4. Glossary of Terms

The following is a supplementary explanation about the terms used in this document.

- ❑ B2B  
Board-to-Board
- ❑ User Board  
Mother board designed by user which is equipped with TB-7Z-IAE
- ❑ Zynq  
Abbreviation of Zynq-7000 All Programmable SoC
- ❑ Zynq PS  
Abbreviation of Zynq Processing System  
A hard macro block containing peripherals based on Zynq's ARM® Cortex™-A9 MPCore™ and memory controller
- ❑ Zynq PL  
Abbreviation of Zynq Programmable Logic  
FPGA fabric (LUT/FF/BRAM/IO/DSP/CMT and others)  
The onboard Zynq is equivalent to Artix®-7 FPGA
- ❑ Industrial Network  
MECHATROLINK-III, CC-Link IE Field, EtherCAT® and others, inclusive of protocols that cannot be realized by IEEE802.3 MAC

## 5. Block Diagram

Figure 5-1 shows a TB-7Z-IAE block diagram.

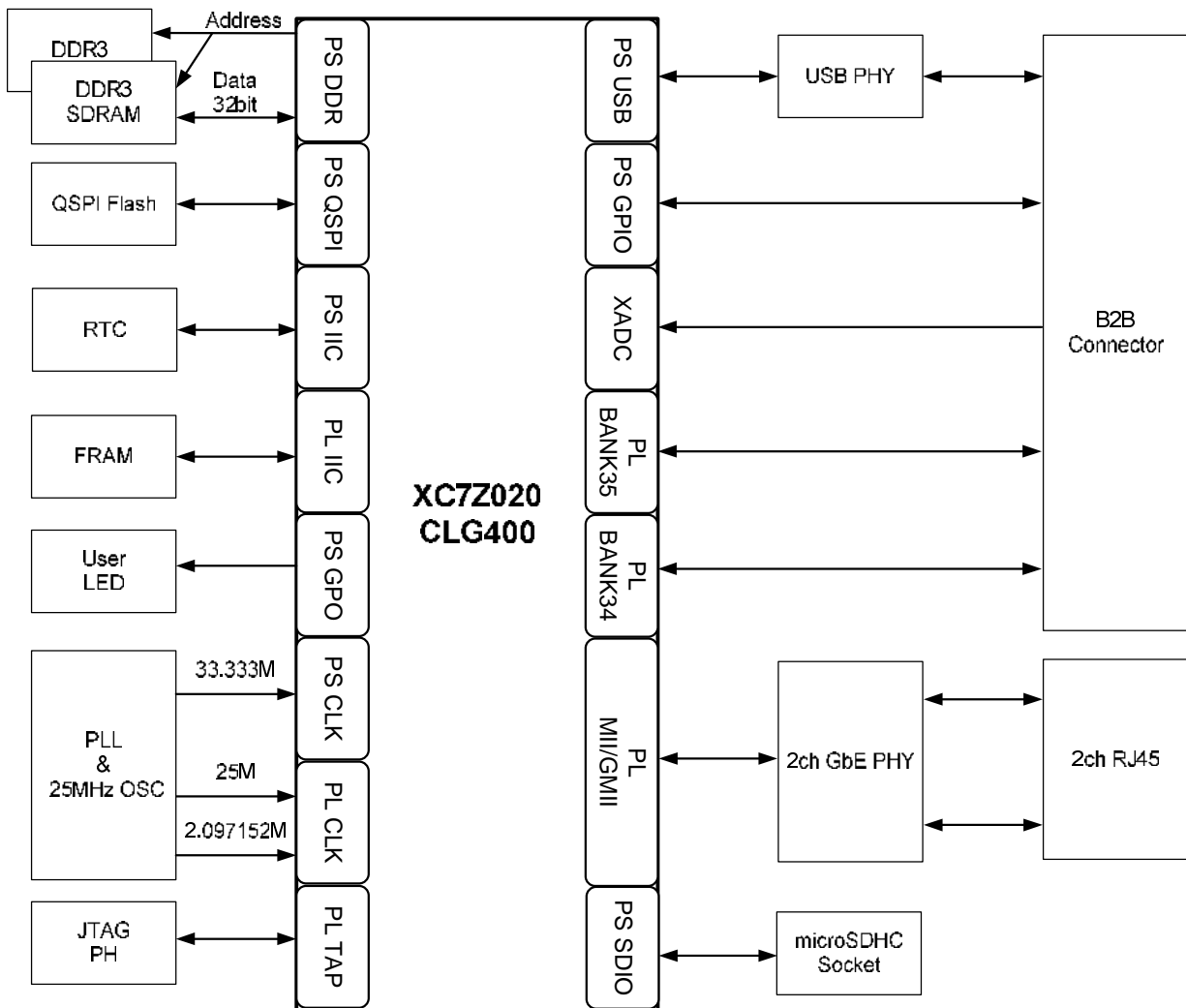


Figure 5-1 TB-7Z-IAE block diagram

## 6. External View of TB-7Z-IAE

Figure 6-1 shows the external view of the TB-7Z-IAE board.

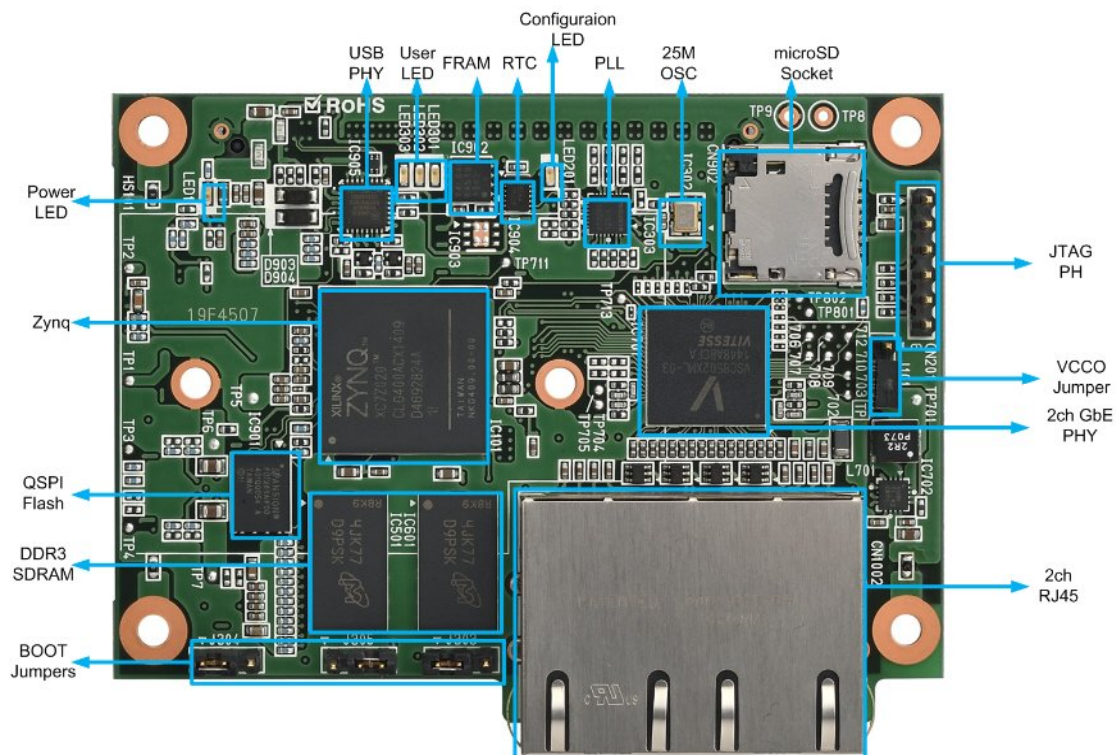


Figure 6-1 Component side

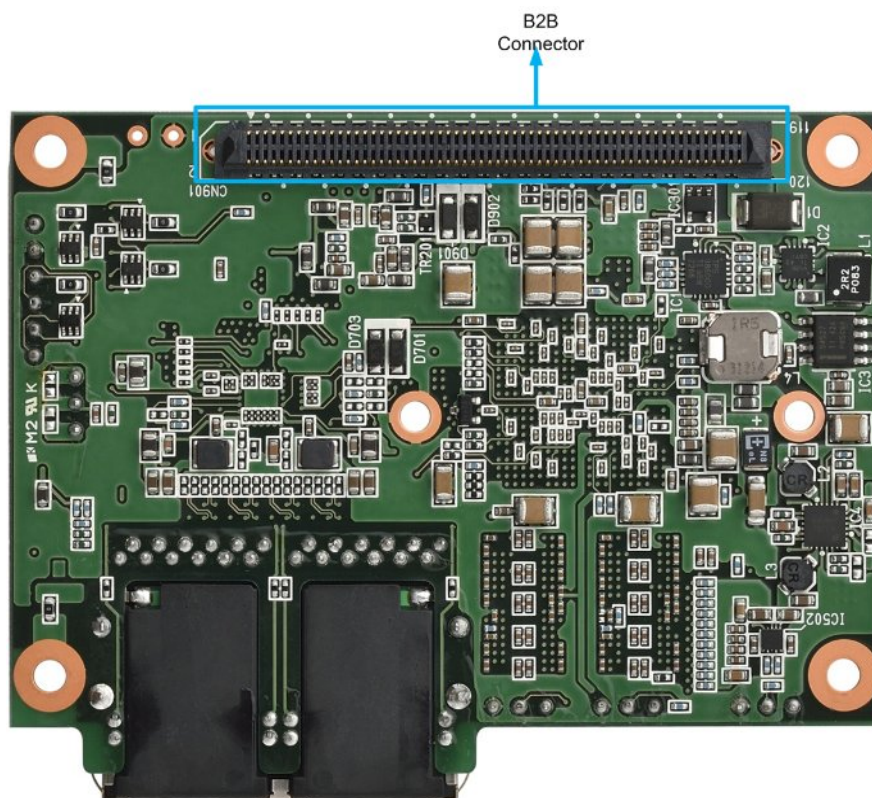


Figure 6-2 Solder side

## 7. Main Specification

Table 7-1 shows the main specification of the TB-7Z-IAE board.

For details and part number, refer to the respective sections.

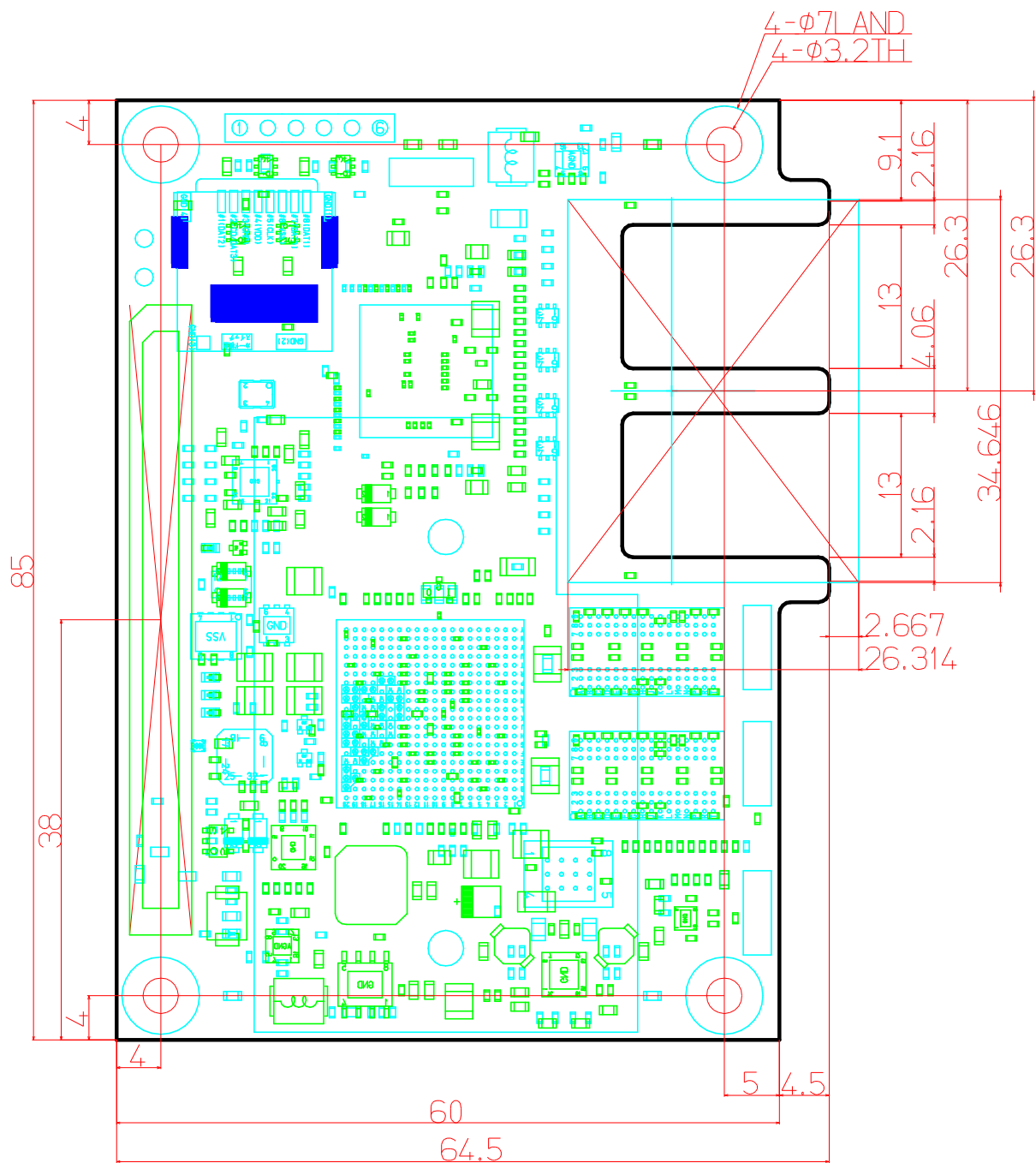
**Table 7-1 Main specification**

Model Number	TB-7Z-IAE
SoC Device	Zynq AP SoC
Memory	512MByte SDRAM 1,066Mbps
	16MByte NOR flash memory
	64Kbit Non-volatile F-RAM
B2B Connector	120pin connector 0.80mm pitch
Onboard Peripherals	Gigabit Ethernet x 2
	USB 2.0 x 1 (w/o USB Connector)
	microSD card socket
Debugging Interface	JTAG、LED
Clock Device	PS and PL clock, RTC device
Power Supply	DC 4.9V ~ 5.10V
Size (inclusive of connectors)	67.2mm(W) x 85.0mm(D) x 20.0mm(H)
Junction temperature range	-25 ~ +85
Recommended operating temperature range	0 ~ +50

## 8. Board Specification

**Figure 8-1** shows the TB-7Z-IAE board specification.

External dimensions:	64.5 mm (W) x 85.0 mm (H)
Number of layers:	12 layers, IVH
Board thickness:	1.8 mm
Material:	FR-4
Surface treatment:	Electroless Gold Plating



**Figure 8-1 Board dimensions**

## 9. Address Map

Figure 9-1 shows the TB-7Z-IAE address map.

This address map is a basic setting. It may be changed dependent on the software that will be executed by Zynq.

For the address map actually installed, refer to the reference design manual and information provided from the OS vendor.

Details about address map:

Refer to XILINX “UG585, Zynq-7000 Technical Reference Manual”, Chapter 4.

FFFF FFFF H	PS On-Chip Memory High Address (if mapped) [192 Kbyte]
FFFC 0000 H	Reserved
FDFE FFFF H	PS QSPI Linear Address [16 Mbyte]
FC00 0000 H	Reserved
F8F0 2FFF H	PS CPU Private Registers [6 Mbyte]
F890 0000 H	Reserved
F880 FFFF H	PS System Registers [8 Mbyte]
F800 1000 H	Reserved
F800 0BFF H	PS SLCR [3 Kbyte]
F800 0000 H	Reserved
E02F FFFF H	PS IOP (UART, USB, I2C, SPI, CAN, GPIO, GbE, QSPI, SDIO) [3 Mbyte]
E000 0000 H	Reserved
BFFF FFFF H	PL Peripherals #1 [1 Gbyte]
8000 0000 H	
7FFF FFFF H	PL Peripherals #0 [1 Gbyte]
4000 0000 H	Reserved
1FFF FFFF H	PS DDR3 SDRAM [512 Mbyte]
0004 0000 H	Reserved
0003 FFFF H	PS On-Chip Memory [192 Kbyte]
0000 0000 H	

Figure 9-1 System address map

## 10. Description of Components

### 10.1. Zynq

The TB-7Z-IAE board is equipped with Zynq model number XC7Z020-1CLG400I (industrial grade type). Zynq integrates a FPGA fabric in the ARM SoC. It allows the utilization of diversity of components from high performance processor to user-programmable logic as follows:

- ☐ Design of special interfaces such as industrial network
- ☐ Design of hardware accelerator in cooperation with software

**Table 10-1 Onboard device specification**

Part Number	XC7Z020
Processor Core	Dual ARM Cortex-A9 MPCore with CoreSight™
Processor Extensions	NEON™ & Single / Double Floating Point for each processor
Maximum Frequency	667MHz
L1 Cache	32KByte Instruction, 32KByte Data per processor
L2 Cache	512KByte
Look-Up Tables (LUTs)	53,200
Flip-Flops (FFs)	106,400
Block RAM	560KByte
DSP Slices	220
Package	CLG400
Speed Grade	-1
Temp Grade	Industrial (-40° to 100°)



### 10.1.1. Heat sink (optional)

A dedicated passive heat sink is available as an option.

It can effectively improve the problems of a heat value of the Zynq device. Consult our representative if needed.

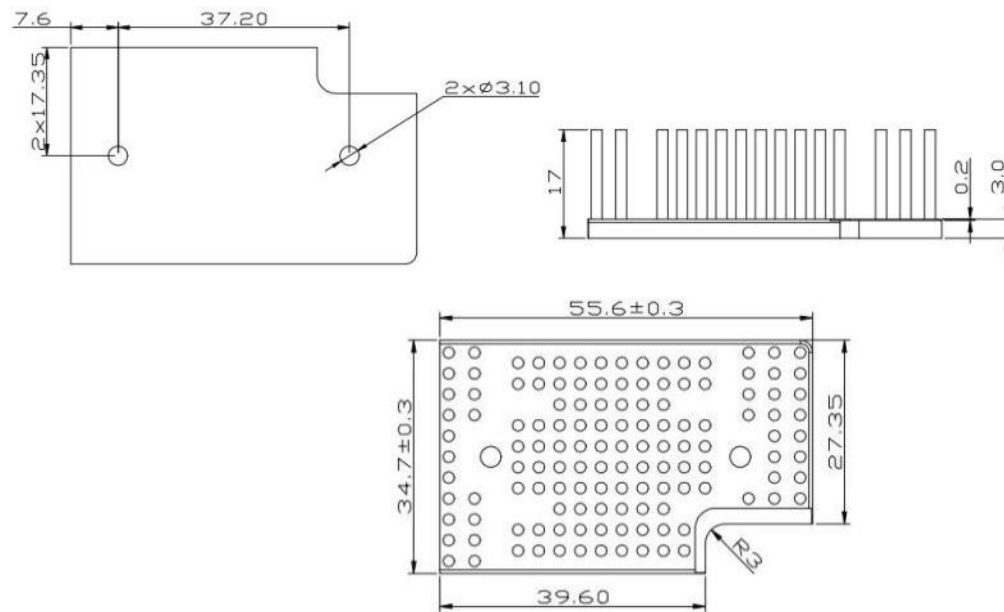


Figure 10-1 Heat sink

Table 10-2 Thermal resistance

	Thermal resistance
LFM	Rth( /W)
30	8.65
50	6.54
80	4.7
200	2.65
400	1.55
600	1.18
800	1.03

### 10.1.2. References

The following lists the Zynq related documents.

1. DS190, Zynq-7000 All Programmable SoC Overview  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds190-Zynq-7000-Overview.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds190-Zynq-7000-Overview.pdf)
2. DS187, Zynq-7000 AP SoC (7010 and 7020): AC and DC Switching Characteristics Data Sheet  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds187-XC7Z010-XC7Z020-Data-Sheet.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds187-XC7Z010-XC7Z020-Data-Sheet.pdf)
3. UG585, Zynq-7000 Technical Reference Manual (TRM)  
[http://www.xilinx.com/support/documentation/user\\_guides/ug585-Zynq-7000-TRM.pdf](http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf)
4. UG865, Zynq-7000 AP SoC Packaging and Pinout Specifications  
[http://www.xilinx.com/support/documentation/user\\_guides/ug865-Zynq-7000-Pkg-Pinout.pdf](http://www.xilinx.com/support/documentation/user_guides/ug865-Zynq-7000-Pkg-Pinout.pdf)
5. UG821, Zynq-7000 AP SoC Software Developers Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug821-zynq-7000-swdev.pdf](http://www.xilinx.com/support/documentation/user_guides/ug821-zynq-7000-swdev.pdf)
6. UG933, Zynq-7000 AP SoC PCB Design and Pin Planning Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug933-Zynq-7000-PCB.pdf](http://www.xilinx.com/support/documentation/user_guides/ug933-Zynq-7000-PCB.pdf)
7. EN247, Zynq-7000 AP SoC Production Errata  
<http://www.xilinx.com/support/documentation/errata/en247.pdf>
8. UG471, 7 Series FPGAs SelectIO Resources User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug471\\_7Series\\_SelectIO.pdf](http://www.xilinx.com/support/documentation/user_guides/ug471_7Series_SelectIO.pdf)
9. UG472, 7 Series FPGAs Clocking Resources User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug585-Zynq-7000-TRM.pdf](http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf)
10. UG473, 7 Series FPGAs Memory Resources User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug473\\_7Series\\_Memory\\_Resources.pdf](http://www.xilinx.com/support/documentation/user_guides/ug473_7Series_Memory_Resources.pdf)
11. UG474, 7 Series FPGAs Configurable Logic Block User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug474\\_7Series\\_CLB.pdf](http://www.xilinx.com/support/documentation/user_guides/ug474_7Series_CLB.pdf)
12. UG479, 7 Series FPGAs DSP48E1 Slice User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug479\\_7Series\\_DSP48E1.pdf](http://www.xilinx.com/support/documentation/user_guides/ug479_7Series_DSP48E1.pdf)
13. UG480, 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug480\\_7Series\\_XADC.pdf](http://www.xilinx.com/support/documentation/user_guides/ug480_7Series_XADC.pdf)
14. UG116, Device Reliability Report  
[http://www.xilinx.com/support/documentation/user\\_guides/ug116.pdf](http://www.xilinx.com/support/documentation/user_guides/ug116.pdf)

## 10.2. Power supply structure

Figure 10-2 shows the power supply structure.

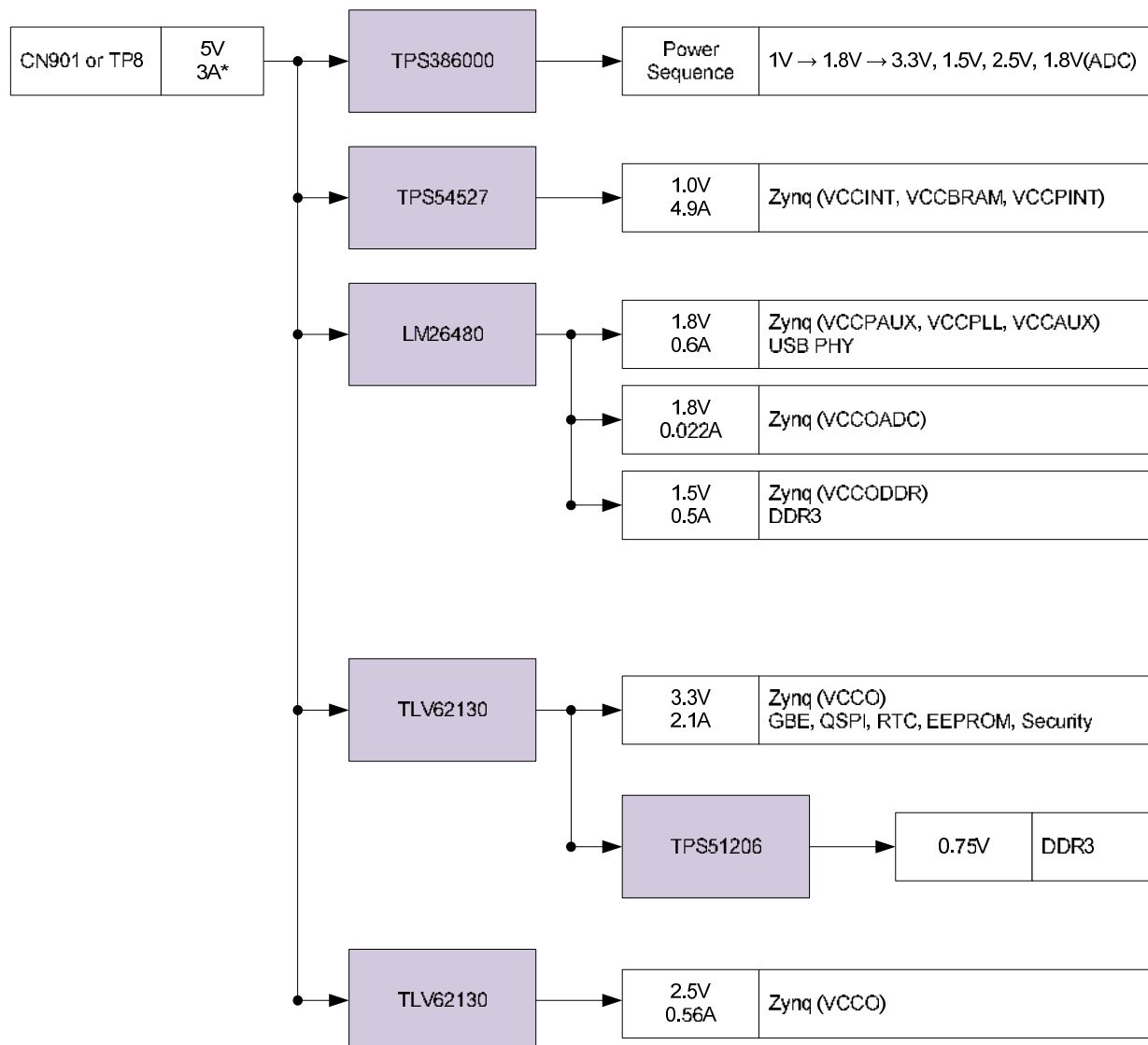
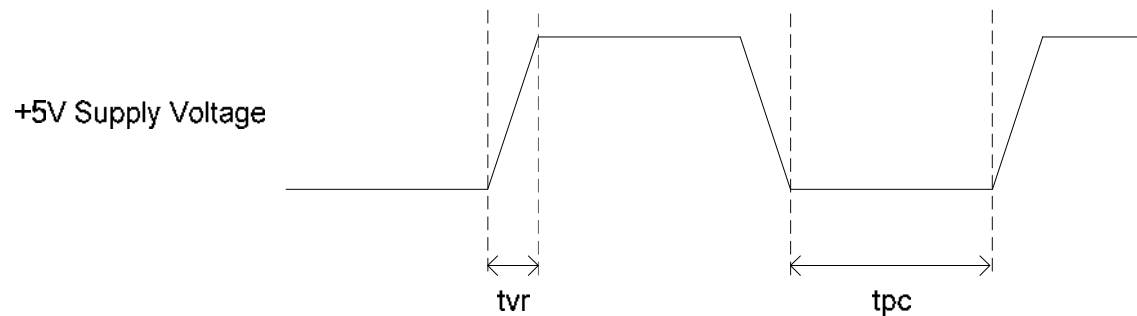


Figure 10-2 Power supply structure

The TB-7Z-IAE has an onboard power supply sequence controller. It can operate on a 5V power supplied through a B2B connector (CN901) from the user board.

If you are outside the input voltage range, The TB-7Z-IAE does not work properly.

If you were once out, asserts the PS\_POR\_B\_MR of B2B connector, please to perform a re-boot.



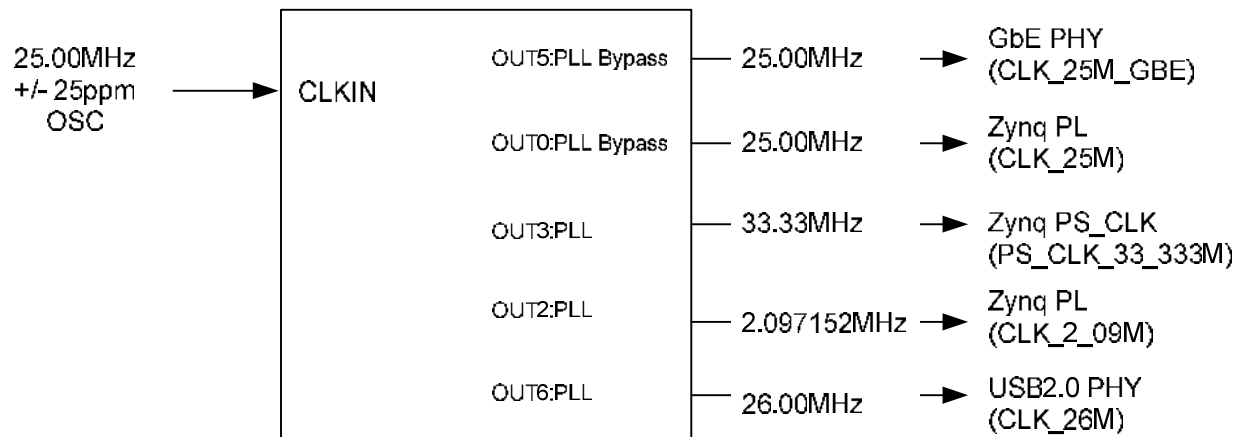
Parameter	Description	Min	Max	Unit
$t_{vr}$	Supply voltage rise time	10	-	msec
$t_{pc}$	Supply voltage cycle off-to-on time	5	-	msec

**Figure 10-3 Recommended +5V supply voltage timing**

### 10.3. Clock structure

The TB-7Z-IAE board has the following clock source (**Figure 10-4**).

The words in parentheses show a signal name.



**Figure 10-4** Clock structure

**Table 10-3** Zynq clock input

PLL Pin No.	Signal Name	Zynq AP SoC Pin	Description
5	CLK_25M_GBE	-	CLK of Ethernet PHY
0	CLK_25M	U18	25MHz Clock for Zynq PL
3	PS_CLK_33_333M	E7	33.333MHz Clock for Zynq PS
2	CLK_2_09M	N18	2.097152MHz Clock for Zynq PL
6	CLK_26M	-	26MHz Clock for USB PHY

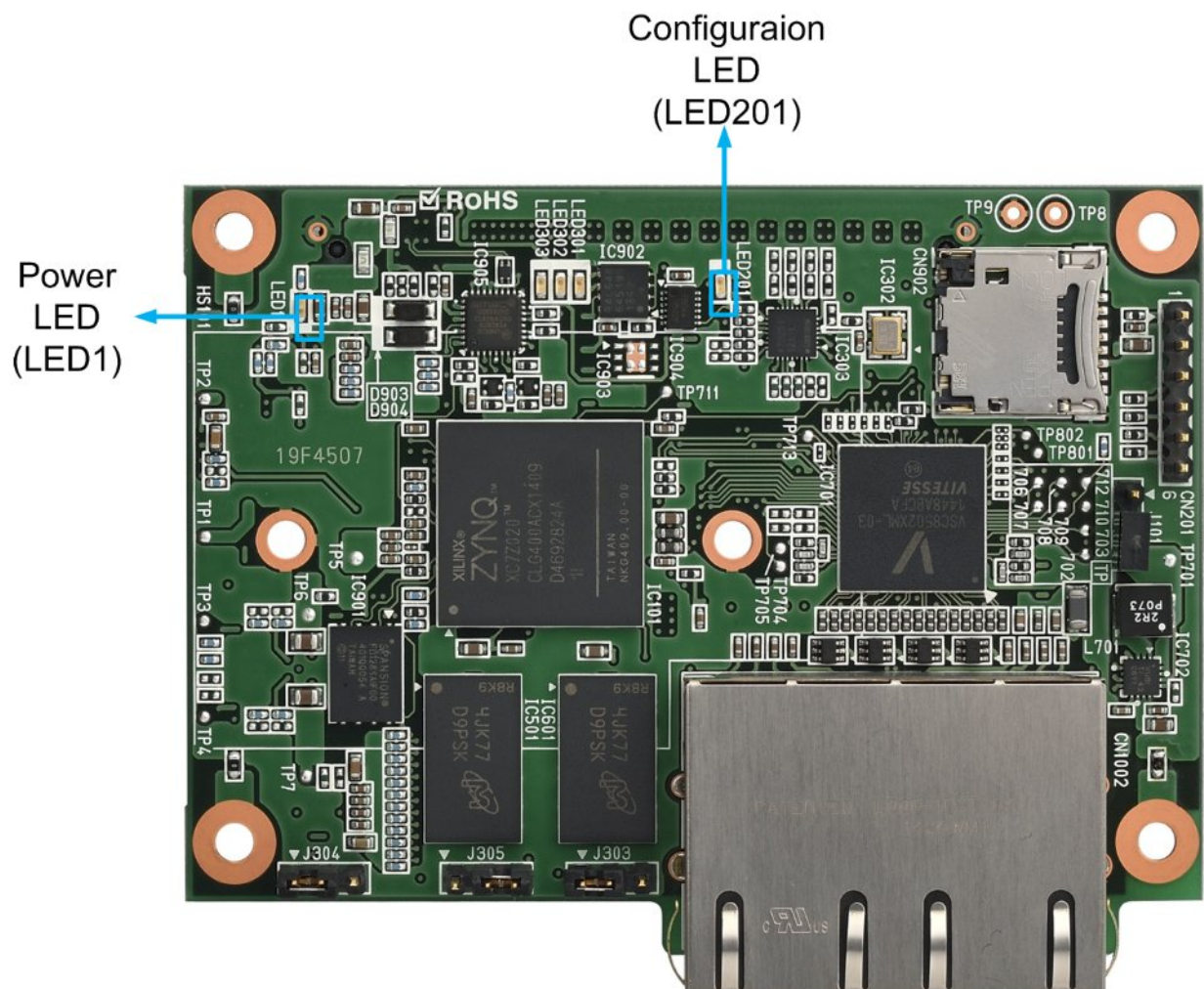
#### 10.4. Board status LED (LED1/LED201)

The current flow from the user board to the TB-7Z-IAE board can be monitored by the onboard LED (LED1).

In addition, the TB-7Z-IAE board also provides another LED (LED201) which shows the completion of Zynq PL configuration after TB-7Z-IAE power up.

**Table 10-4 Board status LED**

Onboard silk	Description
LED1	Yellow. 5V power OK
LED201	Yellow. Completion of Zynq PL configuration



**Figure 10-5 Status LEDs**

### 10.5. B2B connector (CN901)

The TB-7Z-IAE board has one B2B connector on the solder side.

The connector is used to connect the TB-7Z-IAE board and a user board. Hot swapping is not allowed. Zynq PS MIO, Zynq PL IO (2.5/3.3V switchable), Zynq PL IO (3.3V fixed), USB 2.0, XADC input, RTC battery, power supply and ground pin are included.

The following connector (or equivalent) can mate with each other.

- ❑ SAMTEC's ERF8 Series
  - ERF8-060-05.0-L-DV-K-TR
  - ERF8-060-07.0-L-DV-K-TR

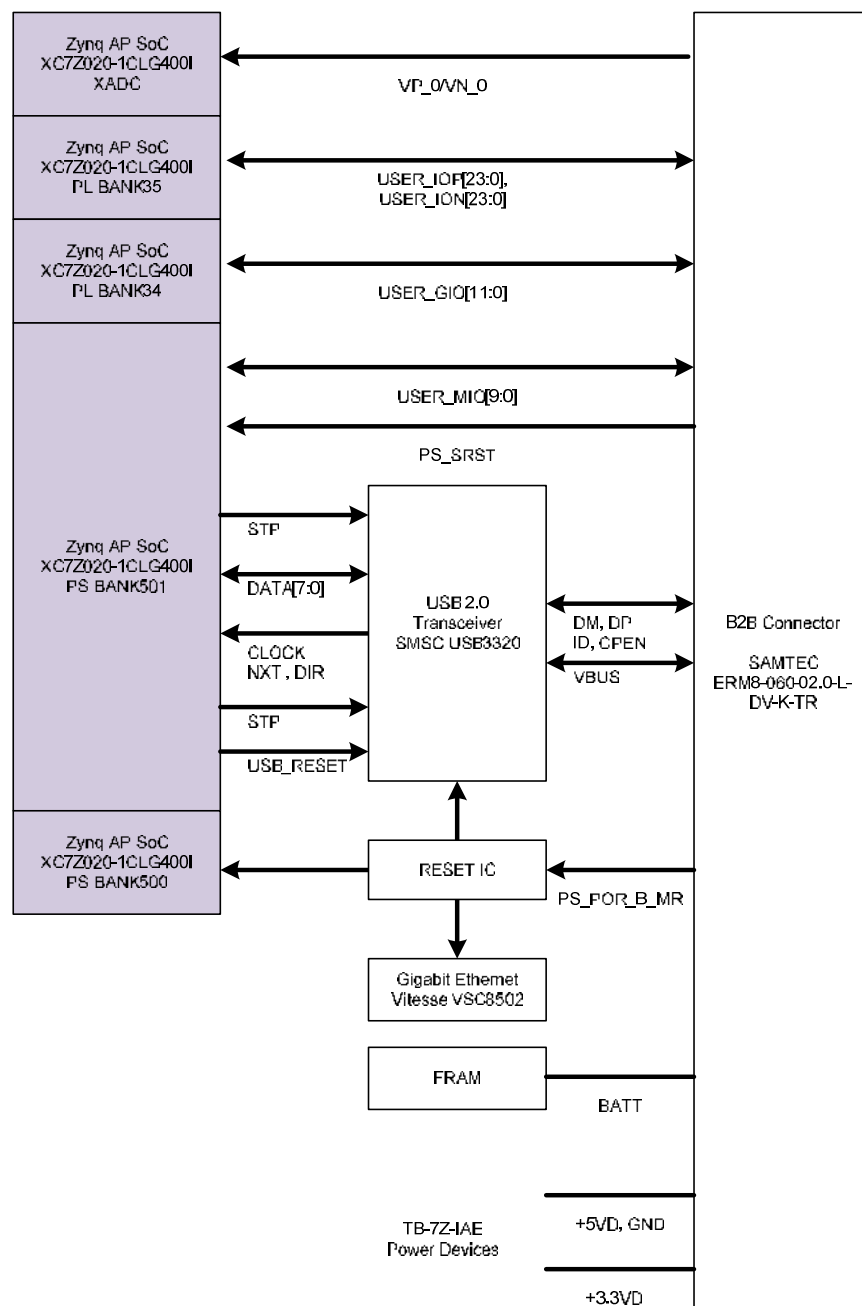
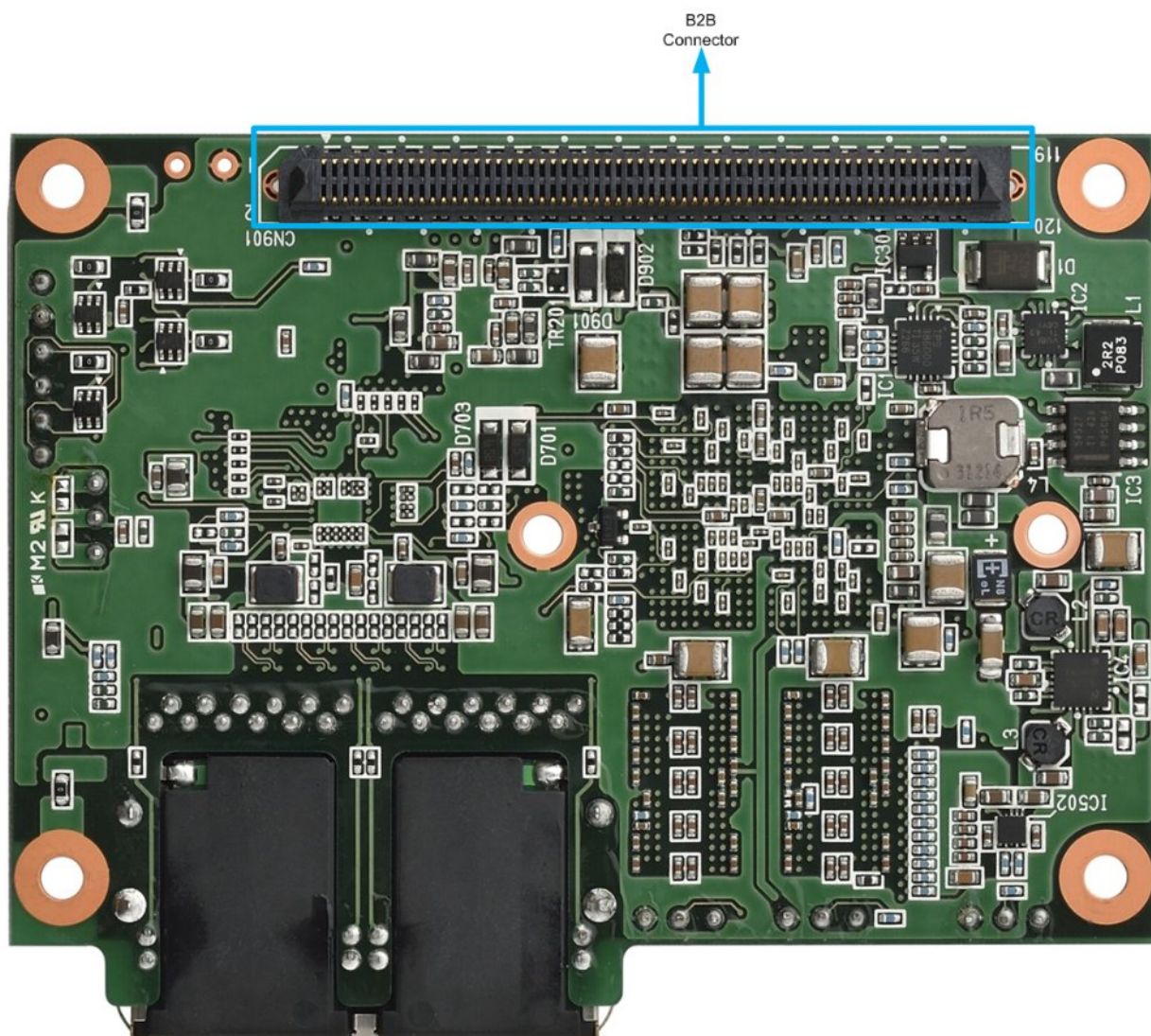


Figure 10-6 B2B connector connecting structure





**Figure 10-7 B2B connector**

Table 10-5 B2B connector pin assignment shows a pin assignment between B2B connector and Zynq.  
 “Dir” shows the signal direction using Zynq as a yardstick.  
 “DIFF P” shows the positive side and “DIFF N” shows the negative side in case of differential signaling.

**Table 10-5 B2B connector pin assignment**

Connect to			Zynq			Description
No.	Signal Name	DIR	Pin LOC	Bank	Level	-
1	DGND	-	-	-	-	Ground
2	DGND	-	-	-	-	Ground
3	USER_IOP00	I/O	K14	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
4	USER_IOP01	I/O	N15	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
5	USER_ION00	I/O	J14	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
6	USER_ION01	I/O	N16	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
7	DGND	-	-	-	-	Ground
8	DGND	-	-	-	-	Ground
9	USER_IOP02	I/O	H16	35	3.3 or 2.5V	Zynq PL IO (DIFF P) MRCC 1



Connect to			Zynq			Description
10	USER_IOP03	I/O	M17	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
11	USER_ION02	I/O	H17	35	3.3 or 2.5V	Zynq PL IO (DIFF N) MRCC 1
12	USER_ION03	I/O	M18	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
13	DGND	-	-	-	-	Ground
14	DGND	-	-	-	-	Ground
15	USER_IOP04	I/O	L14	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
16	USER_IOP05	I/O	M19	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
17	USER_ION04	I/O	L15	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
18	USER_ION05	I/O	M20	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
19	DGND	-	-	-	-	Ground
20	DGND	-	-	-	-	Ground
21	USER_IOP06	I/O	M14	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
22	USER_IOP07	I/O	L19	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
23	USER_ION06	I/O	M15	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
24	USER_ION07	I/O	L20	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
25	DGND	-	-	-	-	Ground
26	DGND	-	-	-	-	Ground
27	USER_IOP08	I/O	L16	35	3.3 or 2.5V	Zynq PL IO (DIFF P) SRCC 1
28	USER_IOP09	I/O	K16	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
29	USER_ION08	I/O	L17	35	3.3 or 2.5V	Zynq PL IO (DIFF N) SRCC 1
30	USER_ION09	I/O	J16	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
31	DGND	-	-	-	-	Ground
32	DGND	-	-	-	-	Ground
33	USER_IOP10	I/O	K17	35	3.3 or 2.5V	Zynq PL IO (DIFF P) MRCC 1
34	USER_IOP11	I/O	K19	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
35	USER_ION10	I/O	K18	35	3.3 or 2.5V	Zynq PL IO (DIFF N) MRCC 1
36	USER_ION11	I/O	J19	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
37	DGND	-	-	-	-	Ground
38	DGND	-	-	-	-	Ground
39	USER_IOP12	I/O	J18	35	3.3 or 2.5V	Zynq PL IO (DIFF P) SRCC 1
40	USER_IOP13	I/O	J20	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
41	USER_ION12	I/O	H18	35	3.3 or 2.5V	Zynq PL IO (DIFF N) SRCC 1
42	USER_ION13	I/O	H20	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
43	DGND	-	-	-	-	Ground
44	DGND	-	-	-	-	Ground
45	USER_IOP14	I/O	G17	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
46	USER_IOP15	I/O	G19	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
47	USER_ION14	I/O	G18	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
48	USER_ION15	I/O	G20	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
49	DGND	-	-	-	-	Ground
50	DGND	-	-	-	-	Ground
51	USER_IOP16	I/O	E17	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
52	USER_IOP17	I/O	F19	35	3.3 or 2.5V	Zynq PL IO (DIFF P)

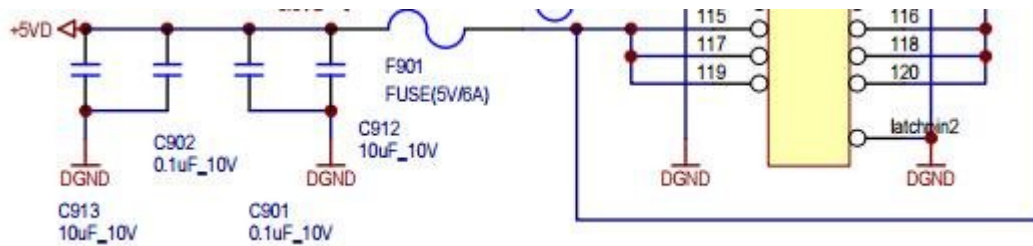
Connect to			Zynq			Description
53	USER_ION16	I/O	D18	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
54	USER_ION17	I/O	F20	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
55	DGND	-	-	-	-	Ground
56	DGND	-	-	-	-	Ground
57	USER_IOP18	I/O	F16	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
58	USER_IOP19	I/O	E18	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
59	USER_ION18	I/O	F17	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
60	USER_ION19	I/O	E19	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
61	DGND	-	-	-	-	Ground
62	DGND	-	-	-	-	Ground
63	USER_IOP20	I/O	B19	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
64	USER_IOP21	I/O	D19	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
65	USER_ION20	I/O	A20	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
66	USER_ION21	I/O	D20	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
67	DGND	-	-	-	-	Ground
68	DGND	-	-	-	-	Ground
69	USER_IOP22	I/O	H15	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
70	USER_IOP23	I/O	C20	35	3.3 or 2.5V	Zynq PL IO (DIFF P)
71	USER_ION22	I/O	G15	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
72	USER_ION23	I/O	B20	35	3.3 or 2.5V	Zynq PL IO (DIFF N)
73	DGND	-	-	-	-	Ground
74	DGND	-	-	-	-	Ground
75	USER_MIO22	I/O	B17	501	3.3V	Zynq PS IO
76	USER_MIO23	I/O	D11	501	3.3V	Zynq PS IO
77	USER_MIO24	I/O	A16	501	3.3V	Zynq PS IO
78	USER_MIO25	I/O	F15	501	3.3V	Zynq PS IO
79	USER_MIO26	I/O	A15	501	3.3V	Zynq PS IO
80	USER_MIO27	I/O	D13	501	3.3V	Zynq PS IO
81	USER_MIO46	I/O	D16	501	3.3V	Zynq PS IO
82	USER_MIO47	I/O	B14	501	3.3V	Zynq PS IO
83	USER_MIO48	I/O	B12	501	3.3V	Zynq PS IO
84	USER_MIO49	I/O	C12	501	3.3V	Zynq PS IO
85	USER_GIO0	I/O	R16	34	3.3V	Zynq PL IO
86	USER_GIO1	I/O	P15	34	3.3V	Zynq PL IO
87	USER_GIO2	I/O	T17	34	3.3V	Zynq PL IO
88	USER_GIO3	I/O	W16	34	3.3V	Zynq PL IO
89	USER_GIO4	I/O	W18	34	3.3V	Zynq PL IO
90	USER_GIO5	I/O	V17	34	3.3V	Zynq PL IO
91	USER_GIO6	I/O	V18	34	3.3V	Zynq PL IO
92	USER_GIO7	I/O	W19	34	3.3V	Zynq PL IO
93	USER_GIO8	I/O	R18	34	3.3V	Zynq PL IO
94	USER_GIO9	I/O	R17	34	3.3V	Zynq PL IO
95	USER_GIO10	I/O	N17	34	3.3V	Zynq PL IO

Connect to			Zynq			Description
96	USER_GPIO11	I/O	P18	34	3.3V	Zynq PL IO
97	DGND	-	-	-	-	Ground
98	DGND	-	-	-	-	Ground
99	PS_POR_B_MR	I	C7	500	3.3V	Reset IC Zynq Power On Reset (Active Low)
100	USB_CPEN	O	-	-	-	External 5V supply Enable for USB.
101	PS_SRST	I	B10	501	3.3V	Zynq System Reset (Active Low)
102	USB_VBUS	Power	-	-	-	VBUS pin of the USB Cable
103	DGND	-	-	-	-	Ground
104	USB_ID	I	-	-	-	ID pin of the USB Cable
105	VP_0	I	K9	0		Zynq XADC analog input (DIFF P)
106	DGND	-	-	-	-	Ground
107	VN_0	I	L10	0		Zynq XADC analog input (DIFF N)
108	USB_DP	IO	-	-	-	D+ pin of the USB Cable
109	DGND	-	-	-	-	Ground
110	USB_DM	IO	-	-	-	D- pin of the USB Cable
111	BATT	Power	-	-	-	RTC Battery
112	DGND	-	-	-	-	Ground
113	+3.3VD	Power	-	-	-	3.3V Output (up to 100mA)
114	+5VD	Power	-	-	-	Board Supply
115	+5VD	Power	-	-	-	Board Supply
116	+5VD	Power	-	-	-	Board Supply
117	+5VD	Power	-	-	-	Board Supply
118	+5VD	Power	-	-	-	Board Supply
119	+5VD	Power	-	-	-	Board Supply
120	+5VD	Power	-	-	-	Board Supply

\* 1 MRCC and SRCC are also used as a clock input pin. If there is a clock output from the user board to Zynq, it is recommended to use this pin. For details, refer to XILINX's **UG472, 7 Series FPGAs Clocking Resources User Guide**.

### 10.5.1. Input power source

The 5V input voltage from the user board is supplied through the B2B connector (CN901) on the reverse side.



**Figure 10-8 Power supply structure**

A repeated power off/on operation at a short interval is not supported.

The TP8 (5V)/TP9 (GND) option is also available which allows 5V input without using a B2B connector. It has soldering structure of through hole for debugging purpose.

**Important: Do not use TP8 and TP9 together with the CN901 power pin.**

### 10.5.2. USER\_IOP00~23, USER\_ION00~23

USER\_IOP00~23/USER\_ION00~23 directly connect the Zynq PL IO and its operation depends on the user circuit.

USER\_IOP00~23/USER\_ION00~23 are designed to cover a wide range of applications from low speed to high speed, for example, maximum rate of 875 Mbps can be realized per pin when utilizing LVDS (low voltage differential signaling).

(In single-end configuration, it targets maximum rate of 148.5Mbps).

Each I/O supports LVCMOS33/LVTTL in 3.3V mode or LVCMOS25/LVDS\_25 in 2.5V mode.

If LVDS\_25 is used, enable the termination of the DIFF\_TERM receiver.

An internal pull-up is enabled from the power-on to the completion of the Zynq PL configuration.

### 10.5.3. I/O voltage selection jumper of USER\_IOP/N (J101)

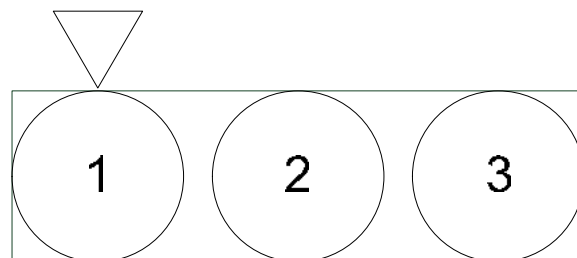
USER\_IOP/N00~23 allows the selection of either 3.3V or 2.5V I/O voltage using J101.

**Table 10-6 I/O voltage setting of USER\_IOP/ION**

VCCO	J101
3.3V	1-2
2.5V	2-3

Figure shows the jumper pin layout.

The position of an onboard triangle mark specifies the pin number 1.



**Figure 10-9 I/O voltage selection pin**

**Important:**

**Turn off the power supply of the TB-7Z-IAE and the user board before performing the selection operation. Otherwise it may cause damage to these boards.**

#### 10.5.4. USER\_GIO0~11

USER\_GIO0~11 directly connect the Zynq PL IO and its operation depends on the user circuit.

They are designed to cover a wide range of applications from low speed to high speed, for example, maximum rate of 100 Mbps can be realized per pin.

Each I/O supports LVCMOS33/LVTTL.

An internal pull-up is enabled from the power-on to the completion of the Zynq PL configuration.

## 10.5.5. USER\_MIO22, 23, 24, 25, 26, 27, 46, 47, 48, 49

These connect the Zynq PS MIO directly, which can be connected to the PS I/O peripheral interface.

In Table 10-7 Connectable PS I/O peripheral interface, the blank area shows the shows the connectable pins.

Table 10-7 Connectable PS I/O peripheral interface

		USER_MIO22	USER_MIO23	USER_MIO24	USER_MIO25	USER_MIO26	USER_MIO27	USER_MIO46	USER_MIO47	USER_MIO48	USER_MIO49
UART0	TX		A				B		C		
	RX	A				B		C			
UART1	TX			D						E	
	RX				D						E
I2C0	SCL	A				B		C			
	SDA		A				B		C		
I2C1	SCL			D						E	
	SDA				D						E
SPI1	MOSI	F						G			
	MISO		F						G		
	SCLK			F						G	
	SS[0]				F						G
CAN0	TX		A				B		C		
	RX	A				B		C			
CAN1	TX			D						E	
	RX				D						E
PJTAG	TDI	H						I			
	TDO		H						I		
	TCK			H						I	
	TMS				H						I
SDIO1	DATA[0]	J									
	CMD		J								
	CLK			J							
	DATA[1]				J						
	DATA[2]					J					
	DATA[3]						J				
GPIO	inout	-	-	-	-	-	-	-	-	-	-

Assignable pin group ("A"~"J" in the table) is predetermined in each PS I/O peripheral interface.

For example, pin assignment across multiple groups (i.e. MIO22 = UART0 RX, MIO27 = UART0 TX) is not permitted. An exception is GPIO. Only specific pin can be assigned to GPIO.

For details, refer to XILINX's **UG585, Zynq-7000 Technical Reference Manual** (Chapter 2).

#### 10.5.6. PS\_POR\_B\_MR, PS\_SRST

It is possible to reset the TB-7Z-IAE Zynq from the user board (negative logic).

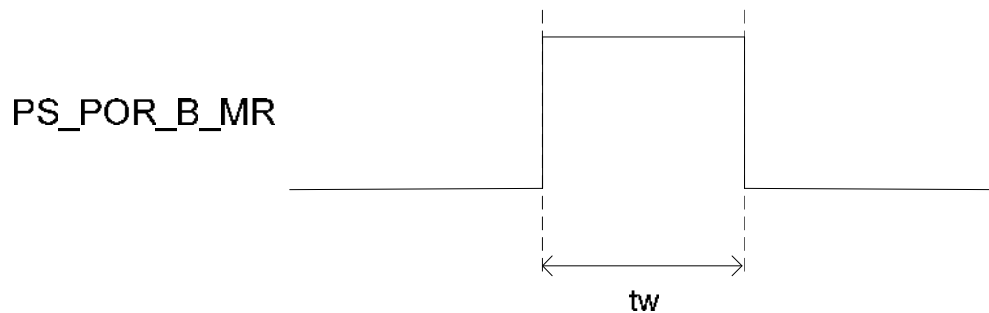
PS\_POR\_B\_MR: Power-on reset

PS\_SRST: System reset

The extent of influence by each reset is as follows:

##### ☐ PS\_POR\_B\_MR

Zynq AP SoC PS\_POR\_B (inclusive of Debug info), USB PHY, Gigabit Ethernet PHY



Parameter	Description	Min	Max	Unit
tw	PS_POR_B_MR pulse width	5	-	μs

**Figure 10-10 PS\_POR\_B\_MR timing**

##### ☐ PS\_SRST

Zynq AP SoC SRST

For details about the influence by each reset, refer to XILINX's **UG585, Zynq-7000 Technical Reference Manual** (Chapter26).

If this reset function is not used on the user board, leave it unconnected. It is pulled up on the TB-7Z-IAE.

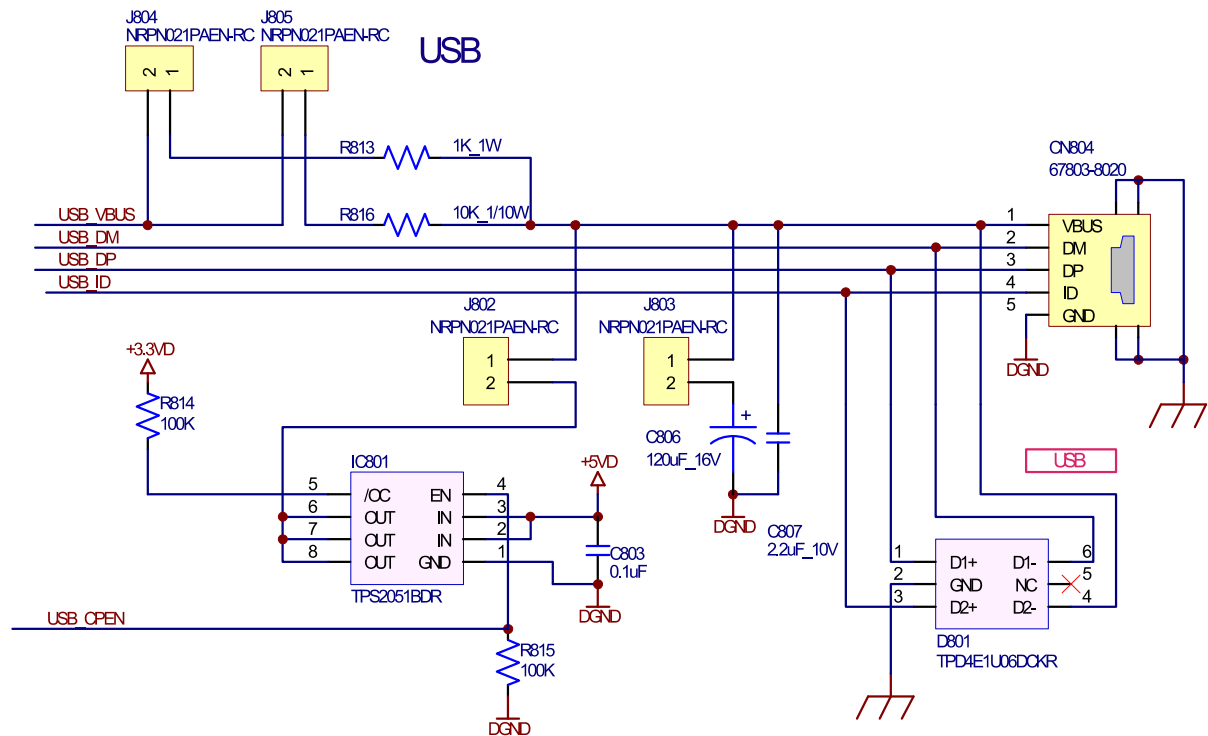


### 10.5.7. USB\_DP, USB\_DM, USB\_CPEN, USB\_VBUS, USB\_ID

This is a signal used to connect the USB PHY (Microchip's USB3320 or equivalent) connected to the Zynq PS on the TB-7Z-IAE to the USB connector on the user board. No need to install the USB PHY on the user board.

Dependent on the design of a user board, it is possible to support HOST, Device or OTG mode.

**Figure 10-11** shows a reference circuit. This circuit allows the selection of HOST, Device or OTG by setting the jumper pin.



**Figure 10-11** Example of user board connection

#### 10.5.8. +3.3VD Output

Pin 113 outputs 3.3V signal from the DCDC on the TB-7Z-IAE board.

**Important:**

In zynq, it is not recommended that the I/O is driven by an external circuit until the device VCCO starts up.

<http://japan.xilinx.com/support/answers/37347.html>

The completion of the VCCO startup can be confirmed by observing that the voltage of Pin 113 reaches 3.3V.

## 10.6. Fixing screw hole

The hole at each corner of the TB-7Z-IAE board can be used as a fixing screw hole to hold a user board.

Screw hole diameter:  $\phi 3.2$

Land diameter:  $\phi 7$

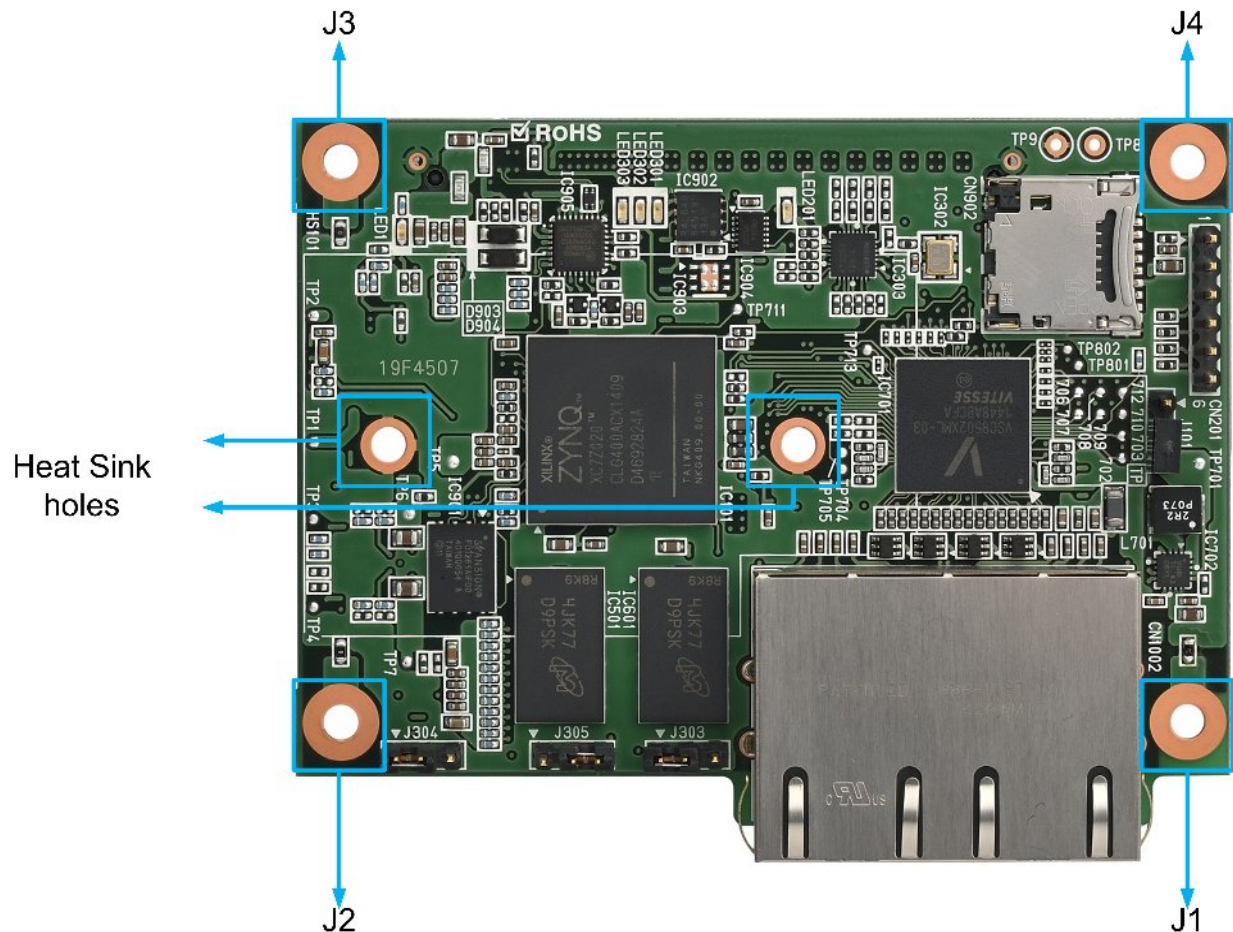


Figure 10-12 TB-7Z-IAE fixing screw hole

Each screw hole has a land connected to a signal ground. One of them is connected to the Fame ground of a RJ connector.

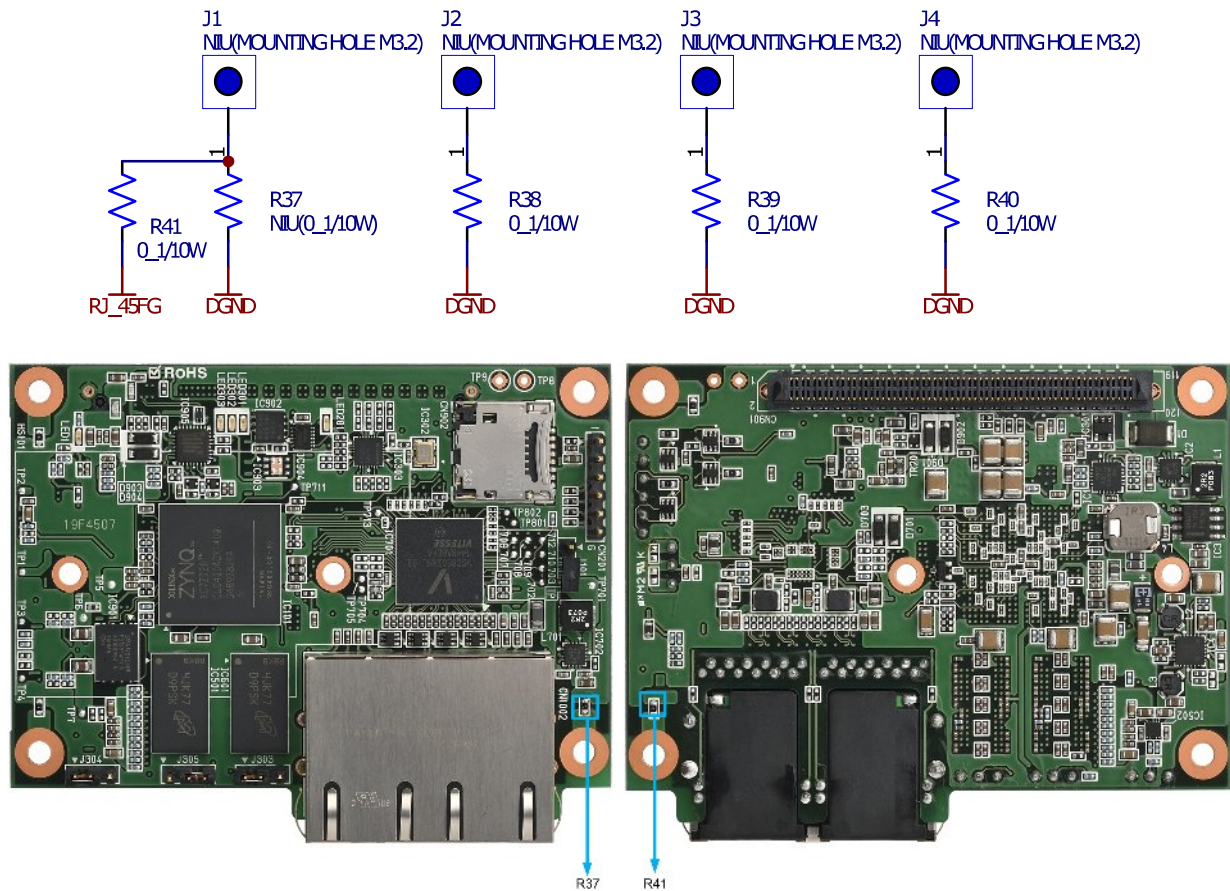
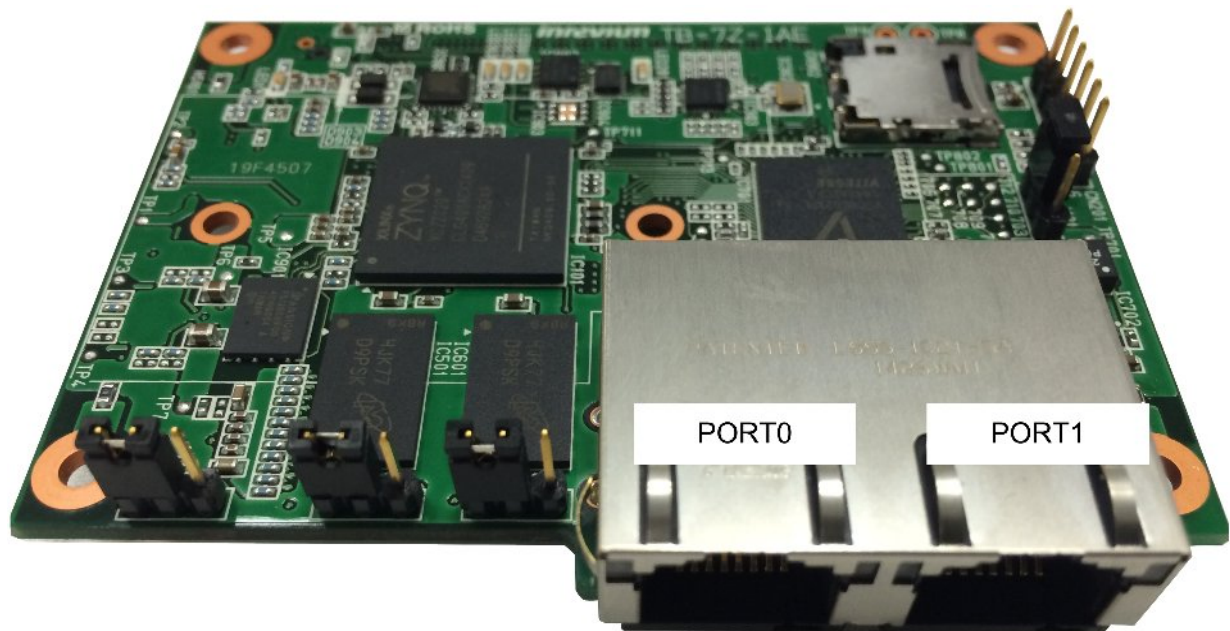


Figure 10-13 Connection between a screw hole and the ground

### 10.7. Gigabit Ethernet ( CN1002 )

The TB-7Z-IAE board is equipped with one 2-port Cat.5e RJ-45 connector capable of TIA/EIA-568-B.



**Figure 10-14 RJ45 connector**

This connector cable is hot swappable.

The connector supports 100M/1000Gbps, auto negotiation and auto MDI/MDI-X.

Since the connector is connected to the Zynq PL, it can be used after the completion of PL configuration.

Table 10-7 shows the R-J45 connector pin assignment.

**Table 10-8 R-J45 connector pin assignment**

No.	Signal Name	Dir	Description
1_P1	TRD0+	I/O	TX/RX Channel 0 Positive Signal
2_P1	TRD0-	I/O	TX/RX Channel 0 Negative Signal
3_P1	TRD1+	I/O	TX/RX Channel 1 Positive Signal
4_P1	TRD2+	I/O	TX/RX Channel 2 Positive Signal not used in 10Base-T/100Base-TX mode
5_P1	TRD2-	I/O	TX/RX Channel 2 Negative Signal not used in 10Base-T/100Base-TX mode
6_P1	TRD1-	I/O	TX/RX Channel 1 Negative Signal
7_P1	TRD3+	I/O	TX/RX Channel 3 Positive Signal not used in 10Base-T/100Base-TX mode
8_P1	TRD3-	I/O	TX/RX Channel 3 Negative Signal not used in 10Base-T/100Base-TX mode
1_P2	TRD0+	I/O	TX/RX Channel 0 Positive Signal
2_P2	TRD0-	I/O	TX/RX Channel 0 Negative Signal
3_P2	TRD1+	I/O	TX/RX Channel 1 Positive Signal
4_P2	TRD2+	I/O	TX/RX Channel 2 Positive Signal not used in 10Base-T/100Base-TX mode
5_P2	TRD2-	I/O	TX/RX Channel 2 Negative Signal not used in 10Base-T/100Base-TX mode
6_P2	TRD1-	I/O	TX/RX Channel 1 Negative Signal
7_P2	TRD3+	I/O	TX/RX Channel 3 Positive Signal not used in 10Base-T/100Base-TX mode
8_P2	TRD3-	I/O	TX/RX Channel 3 Negative Signal not used in 10Base-T/100Base-TX mode

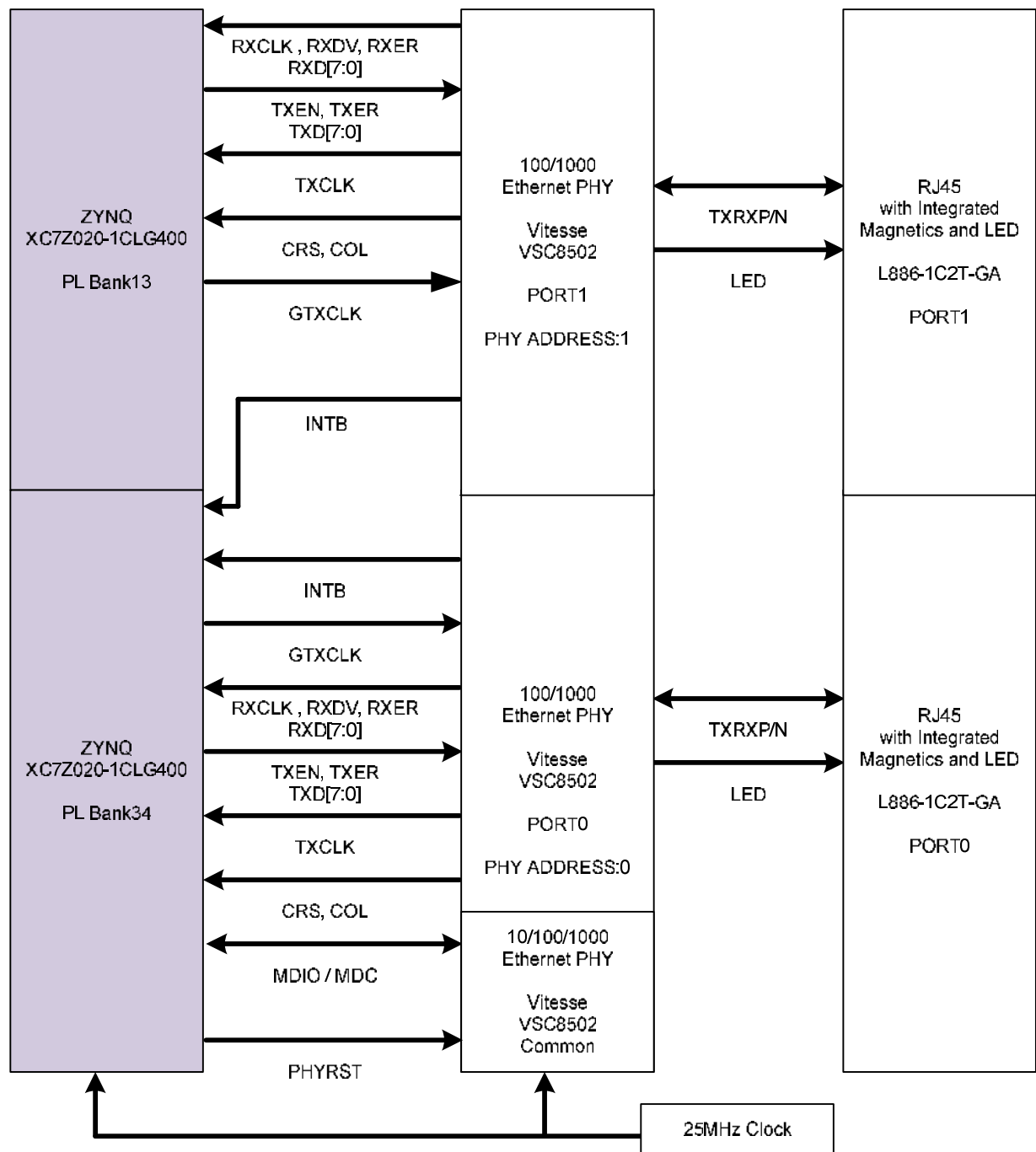


Figure 10-15 Gigabit Ethernet peripherals



Table 10-9 shows the Zynq pin assignment.

**Table 10-9 Zynq - Ethernet PHY pin assignment**

Connect to		Zynq				Description
No.	Signal Name	DIR	Pin LOC	Bank	Level	-
1	GBE_MDIO	I/O	T20	34	3.3V	Management data IO of Gigabit Ethernet Ch0/1
2	GBE_MDC	O	U20	34	3.3V	Management data clock of Gigabit Ethernet Ch0 and 1
3	GBE1_PHYRST	O	P19	34	3.3V	PHY Reset of Gigabit Ethernet Ch1
4	GBE1_TXEN	O	U10	13	3.3V	TX enable of Gigabit Ethernet Ch1
5	GBE1_TXER	O	V5	13	3.3V	TX error of Gigabit Ethernet Ch1
6	GBE1_TXD0	O	Y7	13	3.3V	TX data0 of Gigabit Ethernet Ch1
7	GBE1_TXD1	O	Y6	13	3.3V	TX data1 of Gigabit Ethernet Ch1
8	GBE1_TXD2	O	Y9	13	3.3V	TX data2 of Gigabit Ethernet Ch1
9	GBE1_TXD3	O	Y8	13	3.3V	TX data3 of Gigabit Ethernet Ch1
10	GBE1_TXD4	O	V8	13	3.3V	TX data4 of Gigabit Ethernet Ch1
11	GBE1_TXD5	O	W8	13	3.3V	TX data5 of Gigabit Ethernet Ch1
12	GBE1_TXD6	O	W10	13	3.3V	TX data6 of Gigabit Ethernet Ch1
13	GBE1_TXD7	O	W9	13	3.3V	TX data7 of Gigabit Ethernet Ch1
14	GBE1_GTX_CLK	O	V7	13	3.3V	TX reference clock of Gigabit Ethernet Ch1
15	GBE1_TXCLK	I	U7	13	3.3V	TX clock of Gigabit Ethernet Ch1
16	GBE1_RXCLK	I	T9	13	3.3V	RX clock of Gigabit Ethernet Ch1
17	GBE1_RXER	I	W11	13	3.3V	RX error of Gigabit Ethernet Ch1
18	GBE1_RXDV	I	Y11	13	3.3V	RX data valid of Gigabit Ethernet Ch1
19	GBE1_RXD0	I	T5	13	3.3V	RX data0 of Gigabit Ethernet Ch1
20	GBE1_RXD1	I	U5	13	3.3V	RX data1 of Gigabit Ethernet Ch1
21	GBE1_RXD2	I	Y12	13	3.3V	RX data2 of Gigabit Ethernet Ch1
22	GBE1_RXD3	I	Y13	13	3.3V	RX data3 of Gigabit Ethernet Ch1
23	GBE1_RXD4	I	V11	13	3.3V	RX data4 of Gigabit Ethernet Ch1
24	GBE1_RXD5	I	V10	13	3.3V	RX data5 of Gigabit Ethernet Ch1
25	GBE1_RXD6	I	V6	13	3.3V	RX data6 of Gigabit Ethernet Ch1
26	GBE1_RXD7	I	W6	13	3.3V	RX data7 of Gigabit Ethernet Ch1
27	GBE1_CRS	I	U9	13	3.3V	Carrier sense of Gigabit Ethernet Ch1
28	GBE1_COL	I	U8	13	3.3V	Collision detected of Gigabit Ethernet Ch1
29	GBE_MDINT_1	I	W20	34	3.3V	PHY Interrupt of Gigabit Ethernet Ch1
31	GBE0_PHYRST	O	U19	34	3.3V	PHY Reset of Gigabit Ethernet Ch0
32	GBE0_TXEN	O	R19	34	3.3V	TX enable of Gigabit Ethernet Ch0
33	GBE0_TXER	O	T15	34	3.3V	TX error of Gigabit Ethernet Ch0
34	GBE0_TXD0	O	T11	34	3.3V	TX data0 of Gigabit Ethernet Ch0
35	GBE0_TXD1	O	T10	34	3.3V	TX data1 of Gigabit Ethernet Ch0
36	GBE0_TXD2	O	T12	34	3.3V	TX data2 of Gigabit Ethernet Ch0
37	GBE0_TXD3	O	U12	34	3.3V	TX data3 of Gigabit Ethernet Ch0
38	GBE0_TXD4	O	V13	34	3.3V	TX data4 of Gigabit Ethernet Ch0
39	GBE0_TXD5	O	V12	34	3.3V	TX data5 of Gigabit Ethernet Ch0
40	GBE0_TXD6	O	W13	34	3.3V	TX data6 of Gigabit Ethernet Ch0



Connect to		Zynq				Description
41	GBE0_TXD7	O	T14	34	3.3V	TX data7 of Gigabit Ethernet Ch0
42	GBE0_GTX_CLK	O	U15	34	3.3V	TX reference clock of Gigabit Ethernet Ch0
43	GBE0_TXCLK	I	U14	34	3.3V	TX clock of Gigabit Ethernet Ch0
44	GBE0_RXCLK	I	N20	34	3.3V	RX clock of Gigabit Ethernet Ch0
45	GBE0_RXDV	I	R14	34	3.3V	RX data valid of Gigabit Ethernet Ch0
46	GBE0_RXER	I	P14	34	3.3V	RX error of Gigabit Ethernet Ch0
47	GBE0_RXD0	I	Y16	34	3.3V	RX data0 of Gigabit Ethernet Ch0
48	GBE0_RXD1	I	Y17	34	3.3V	RX data1 of Gigabit Ethernet Ch0
49	GBE0_RXD2	I	W14	34	3.3V	RX data2 of Gigabit Ethernet Ch0
50	GBE0_RXD3	I	Y14	34	3.3V	RX data3 of Gigabit Ethernet Ch0
51	GBE0_RXD4	I	T16	34	3.3V	RX data4 of Gigabit Ethernet Ch0
52	GBE0_RXD5	I	U17	34	3.3V	RX data5 of Gigabit Ethernet Ch0
53	GBE0_RXD6	I	V15	34	3.3V	RX data6 of Gigabit Ethernet Ch0
54	GBE0_RXD7	I	W15	34	3.3V	RX data7 of Gigabit Ethernet Ch0
55	GBE0_CRS	I	U13	34	3.3V	Carrier sense of Gigabit Ethernet Ch0
56	GBE0_COL	I	P20	34	3.3V	Collision detected of Gigabit Ethernet Ch0
57	GBE_MDINT_0	I	V20	34	3.3V	PHY Interrupt of Gigabit Ethernet Ch0

### 10.8. microSD card socket (CN902)

The TB-7Z-IAE board is equipped with one microSD card socket.

Since all microSD card socket pins are connected to PS, this does not allow a direct connection from PL.

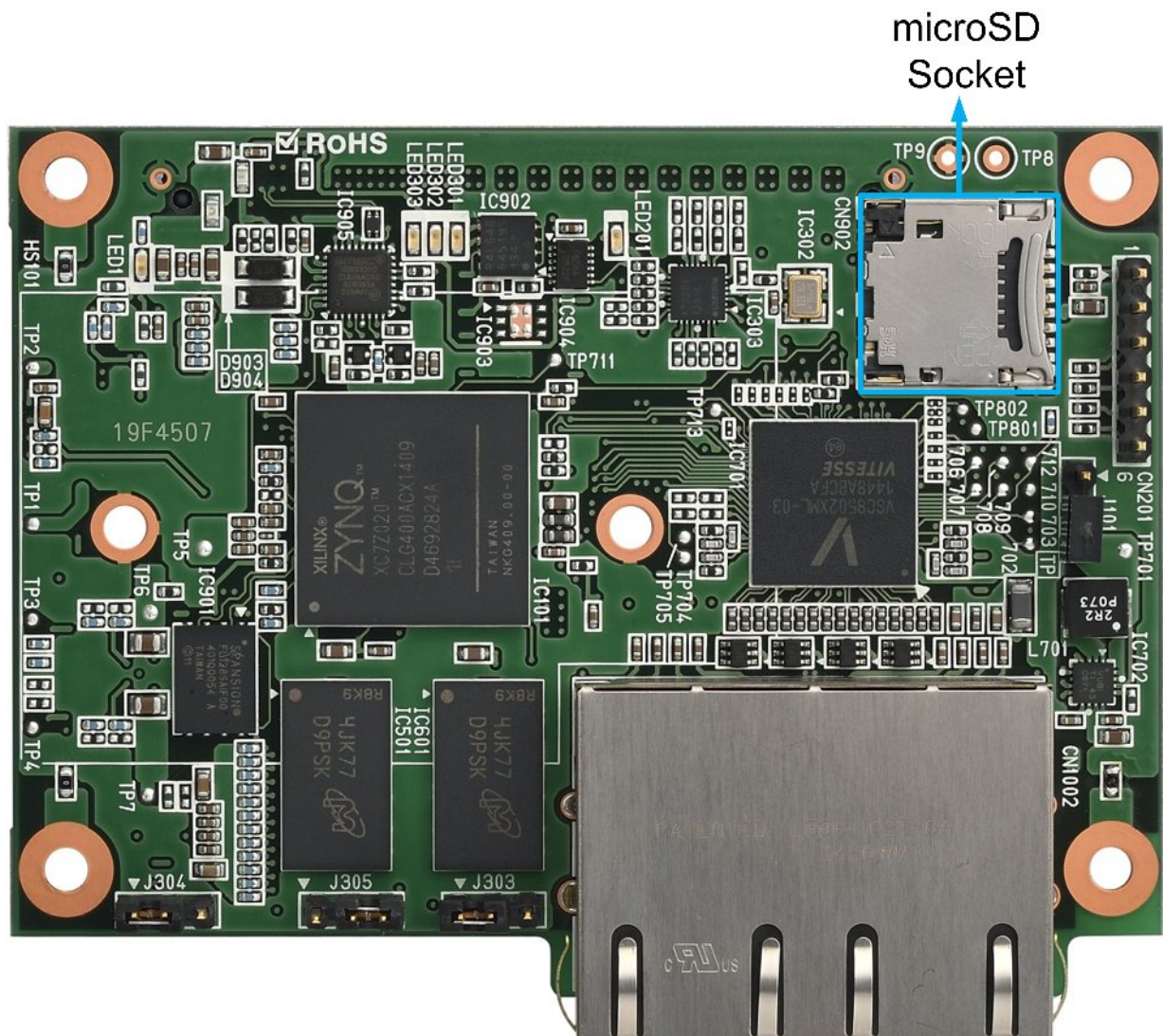


Figure 10-16 microSD card socket

[Operation of this function is confirmed with below.]

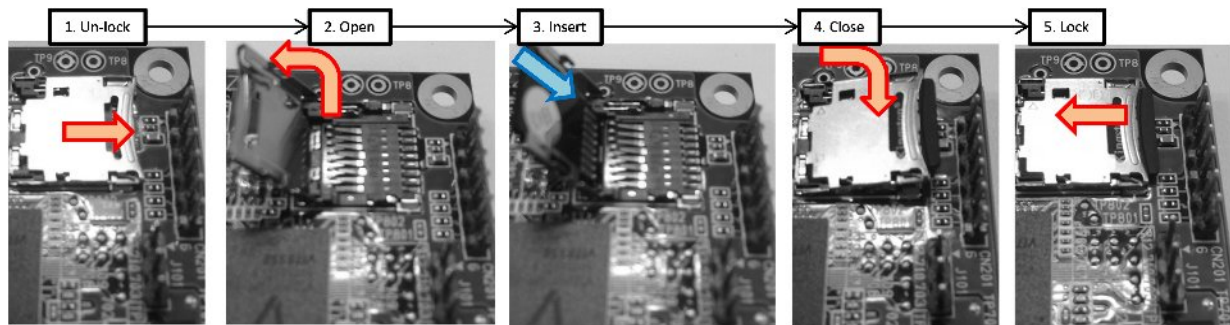
- MSD6-002GK(H00SDI)

The microSD card is not hot-swappable.

Do not apply pressure to any part of the socket when the card is not inserted.

The microSD card socket has a hinge type socket structure for card falling prevention.

Refer to **Figure 10-17** for information on how to insert or remove the microSD card.



**Figure 10-17** Method to insert/remove the microSD card

### 10.9. JTAG connector (CN201)

The TB-7Z-IAE board is equipped with a connector that can connect Xilinx's JTAG cable **HW-USB-II-G**. The JTAG connector is connected to the Zynq TAP controller, allowing access from the JTAG cable to Zynq PS/Zynq PL.

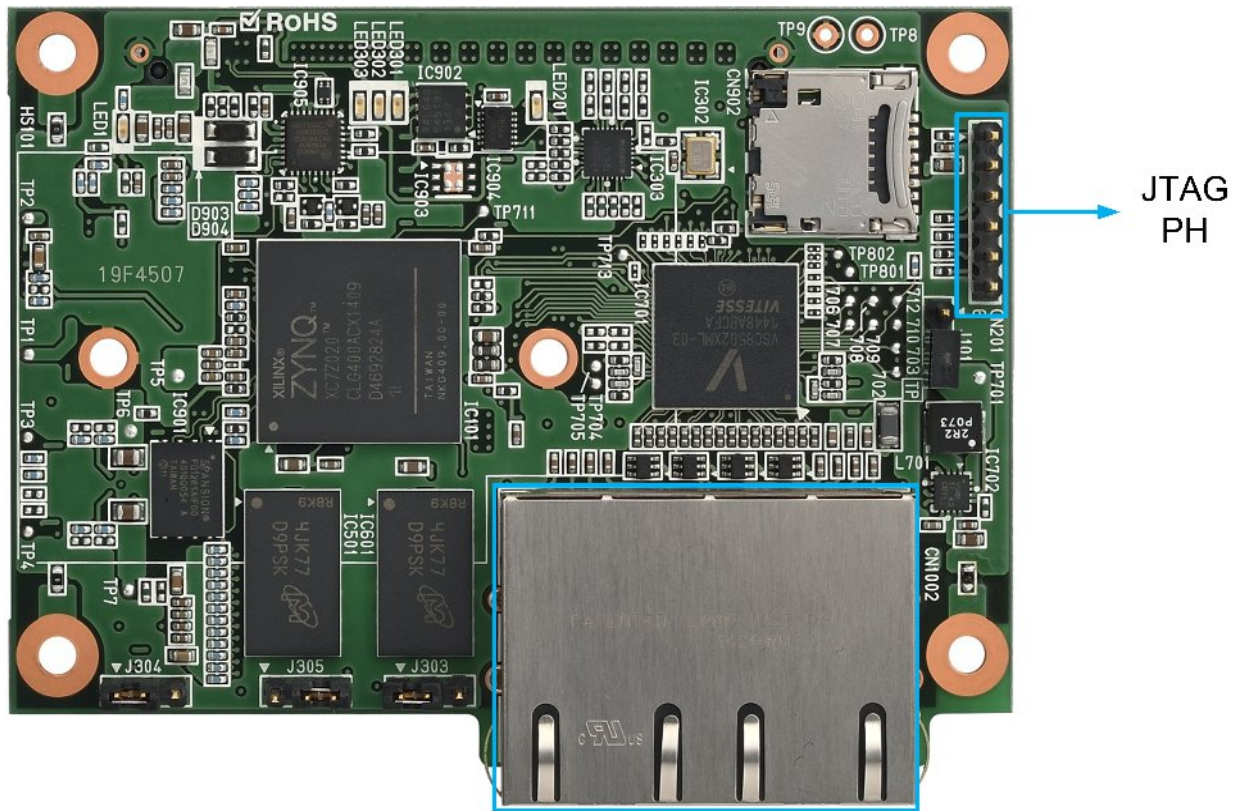


Figure 10-18 JTAG connector

Figure 10-19 shows the JTAG connector pin. Look at the silk number (1,6) at both ends of the connector.

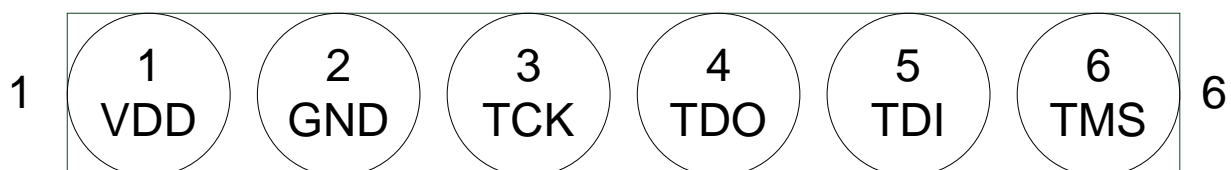


Figure 10-19 JTAG connector pin

If the **HW-USB-II-G** is connected, use the **HW-USB-FLYLEADS-G**.  
DIGILENT's **JTAG HS2 Programming Cable** can also be used instead of the **HW-USB-II-G**.



### 10.10. User LED (LED301/LED302/LED303)

The TB-7Z-IAE board is equipped with 3 user-program controllable LEDs.

Since all pins are connected to PS, this does not allow a direct connection from PL.

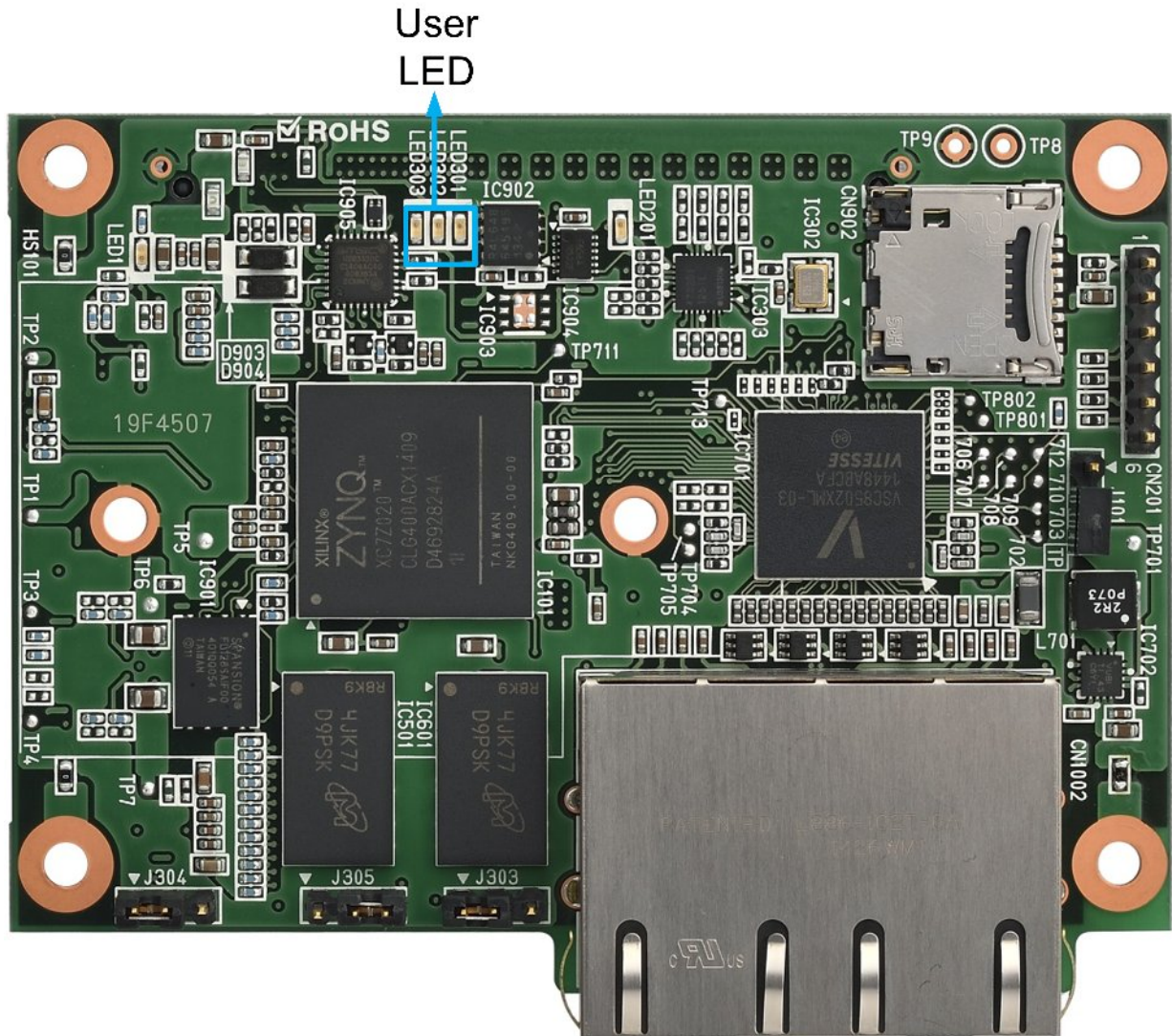


Figure 10-20 User LEDs

Table 10-10 shows the pin assignment between Zynq and LED.

“Dir” shows the signal direction using Zynq as a yardstick. Each LED is turned on when the Zynq output pin is driven “low”.

Table 10-10 Zynq - LED pin assignment

Board Silk	Dir	Zynq Pin	Description
LED301	O	E8	Yellow, Zynq PS GPIO13
LED302	O	C5	Yellow, Zynq PS GPIO14
LED303	O	C8	Red, Zynq PS GPIO15

### 10.11.DDR3 SDRAM

The TB-7Z-IAE board is equipped with 2 DDR3 SDRAMs (Micron's MT41K128M16JT-125 IT:K or equivalent), which are wired in a fly-by topology to the Zynq PS.

They have a 32-bit data bus (shared address and control signal) with total capacity of 512 Mbyte and maximum data rate of 1,066 Mbps.

Since all pins are connected to PS, this does not allow a direct connection from PL.

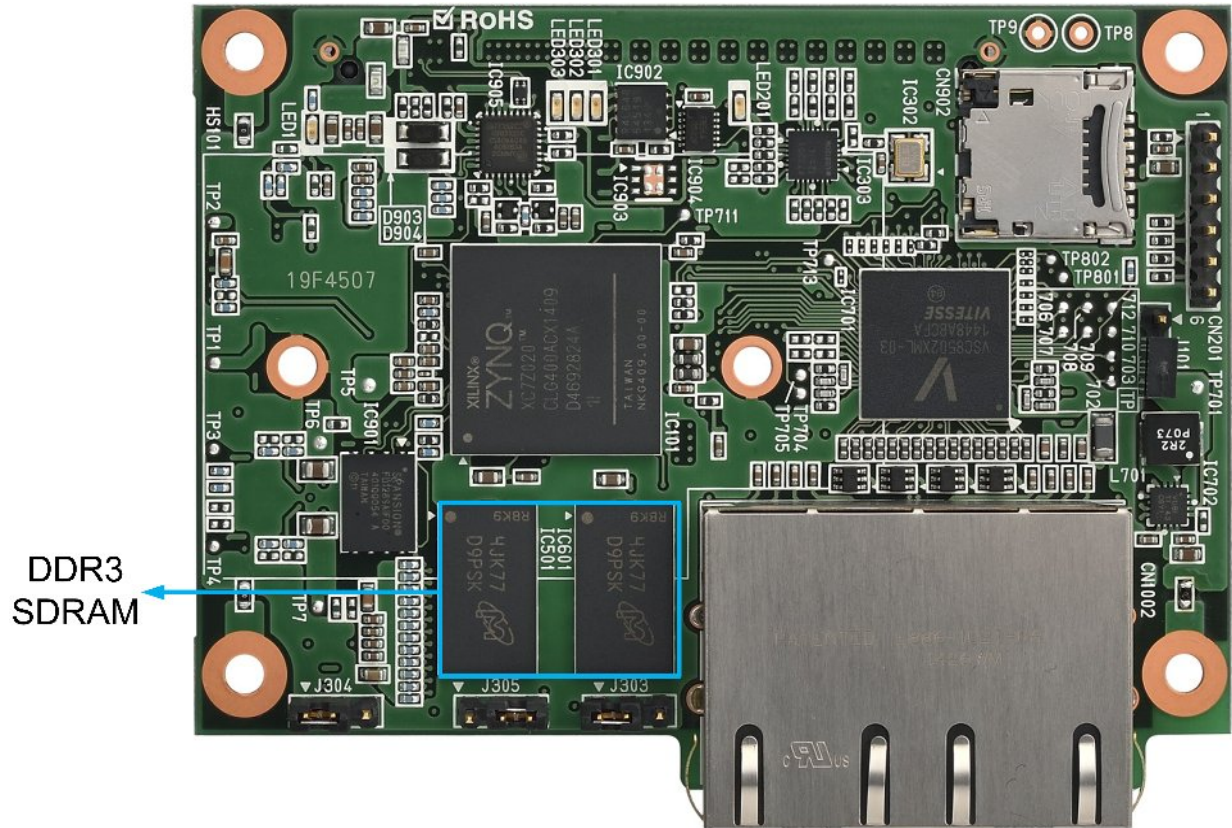


Figure 10-21 DDR3 SDRAM

- ❑ Memory specification  
2Gbit(16M x 16 x 8banks) x 2chip
- ❑ Address structure  
Bank = 3bit  
Address = 15bit (Row address = 15bit / Column address = 10bit)
- ❑ Data bus structure  
Byte access with data strobe signal (DQS), data mask for each byte

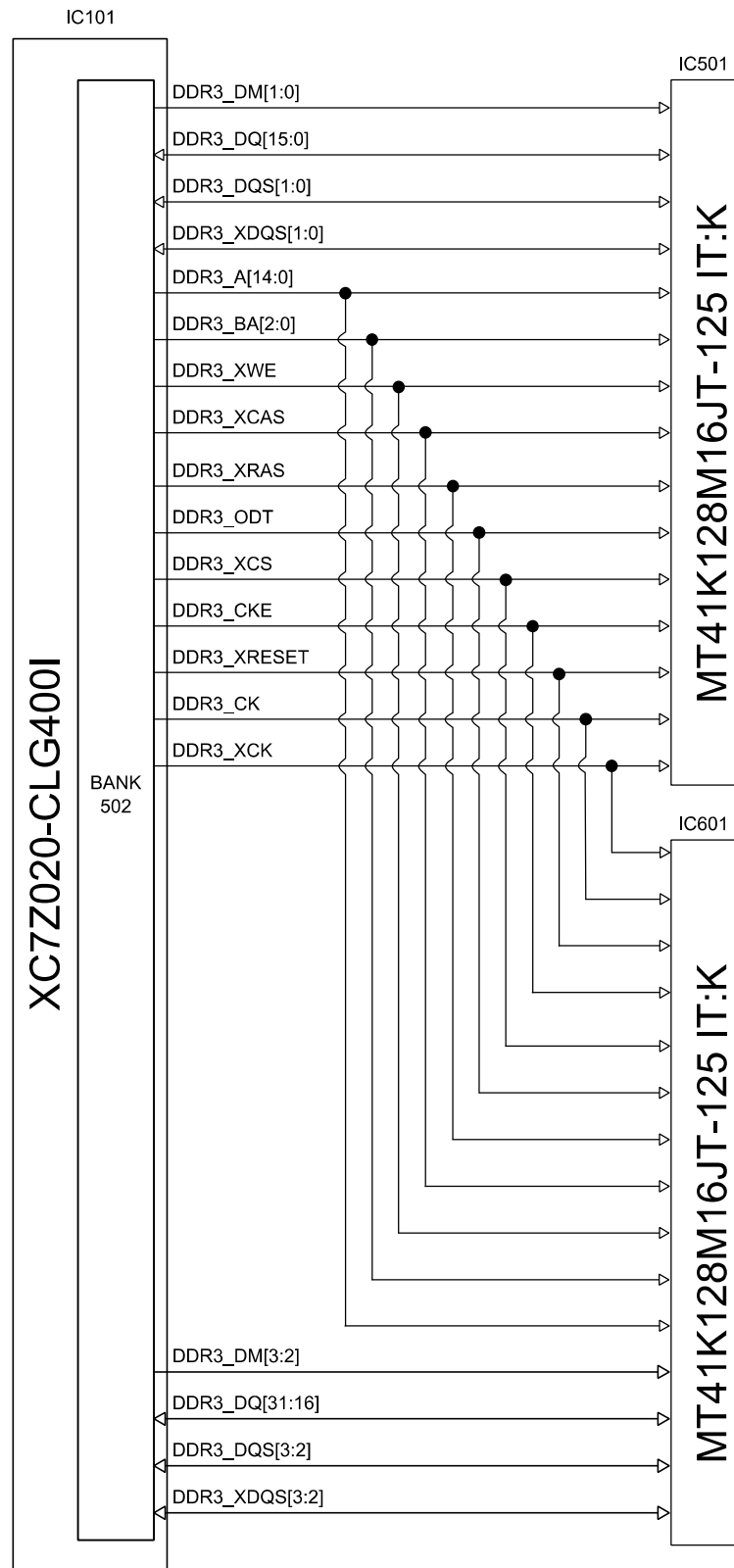


Figure 10-22 DDR3 SDRAM connections



### 10.12.QSPI Flash

The TB-7Z-IAE board has one QSPI NOR Flash Memory (Spansion's S25FL128S or equivalent) connected to Zynq PS.

- ❑ S25FL128S specs
  - Cycling Endurance
    - 100,000 Program-Erase Cycles on any sector typical
  - Data Retention
    - 20 Year Data Retention typical

It is a non-volatile 16 Mbyte memory capable of storing Zynq PL configuration data, OS boot-up data and others.

Since all pins are connected to PS, this does not allow a direct connection from PL.

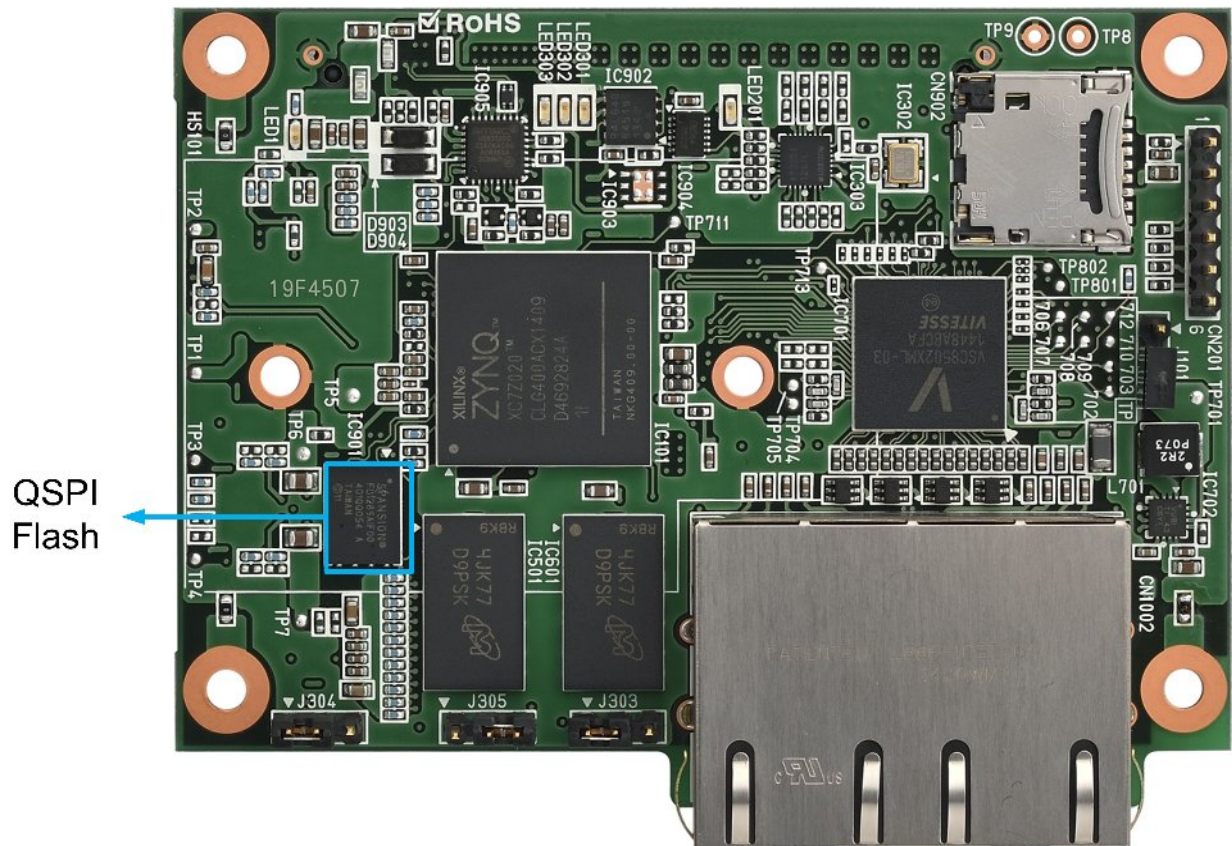


Figure 10-23 QSPI Flash



### 10.13.F-RAM

The TB-7Z-IAE board is equipped with one I2C Nonvolatile F-RAM (Cypress's FM24CL64B or equivalent) connected to Zynq PL.

- ❑ FM24CL64B specs
  - High-endurance 100 trillion (10<sup>14</sup>) read/writes
  - Data retention
    - [Ambient Temperature (TA)]
    - TA=85 : 10-year
    - TA=75 : 38-year
    - TA=65 : 151-year

Since it is connected to Zynq PL, it cannot be used until Zynq PL configuration is completed. It is a non-volatile 16 Mbyte memory capable of storing various data.

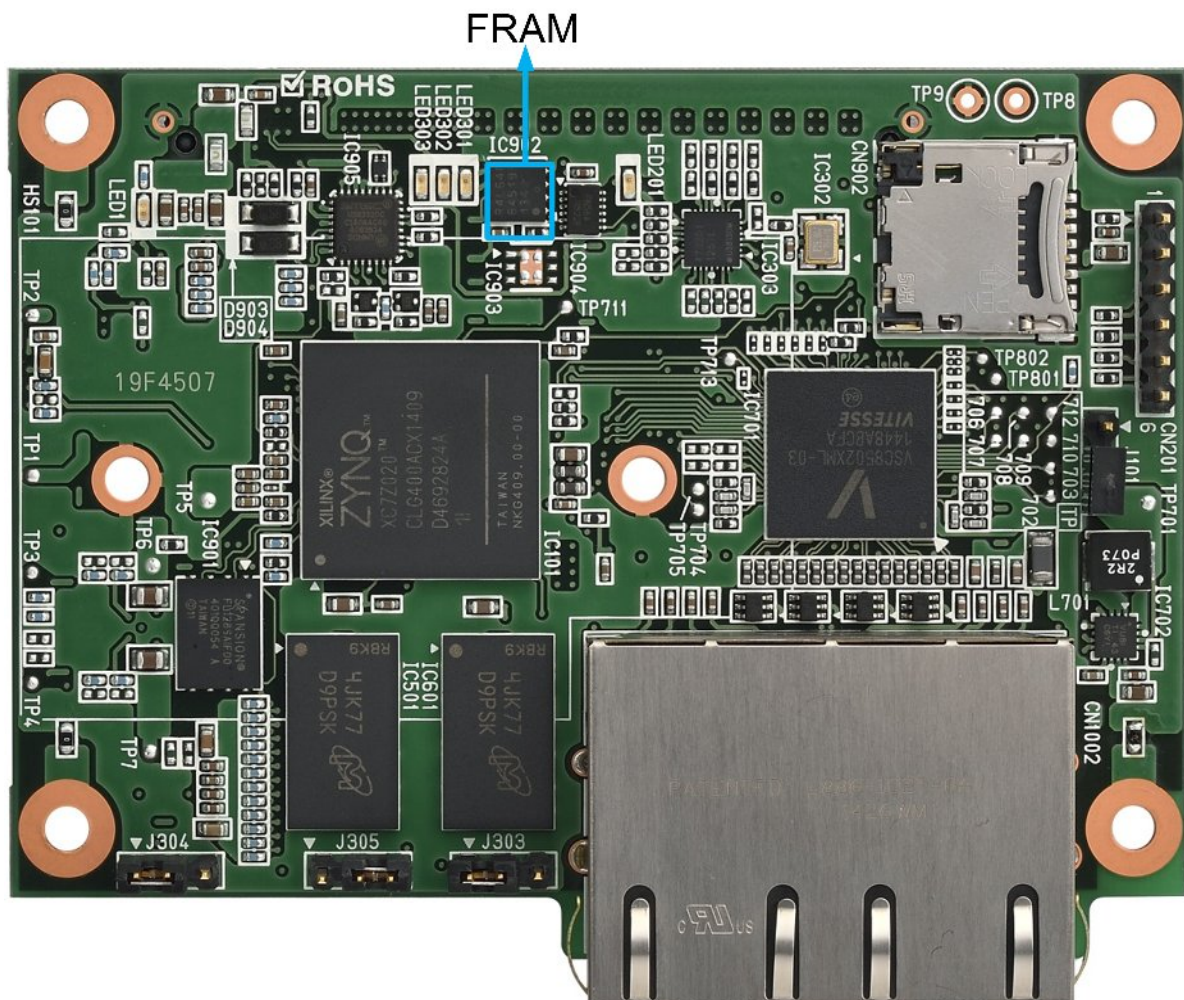


Figure 10-24 F-RAM

I2C slave address is as follows:

- ❑ I2C Write Address: 10100000 (0xA0)
- ❑ I2C Read Address: 10100001 (0xA1)

Table 10-11 shows the pin assignment between F-RAM and Zynq.

“Dir” shows the signal direction using Zynq as a yardstick.

**Table 10-11 Zynq - F-RAM pin assignment**

No.	Signal Name	Dir	Zynq Pin	Description
1	DGND	-	-	F-RAM Address 0
2	DGND	-	-	F-RAM Address 1
3	DGND	-	-	F-RAM Address 2
4	DGND	-	-	F-RAM VSS
5	PL_I2C_SDA	IO	T19	F-RAM Serial data address
6	PL_I2C_SCL	O	P16	F-RAM Serial clock, Fmax 1MHz
7	DGND	-	-	F-RAM Write protect
8	+3.3V	-	-	F-RAM VDD

### 10.14.RTC

The TB-7Z-IAE board is equipped with one real time clock module (Epson's RX-8564LC or equivalent) connected to Zynq PS/I2C. It provides a calendar, a time counter and a constant cycle timer interrupt showing year, month, day, hour, minute, and second.

Since all pins are connected to PS, this does not allow a direct connection from PL.

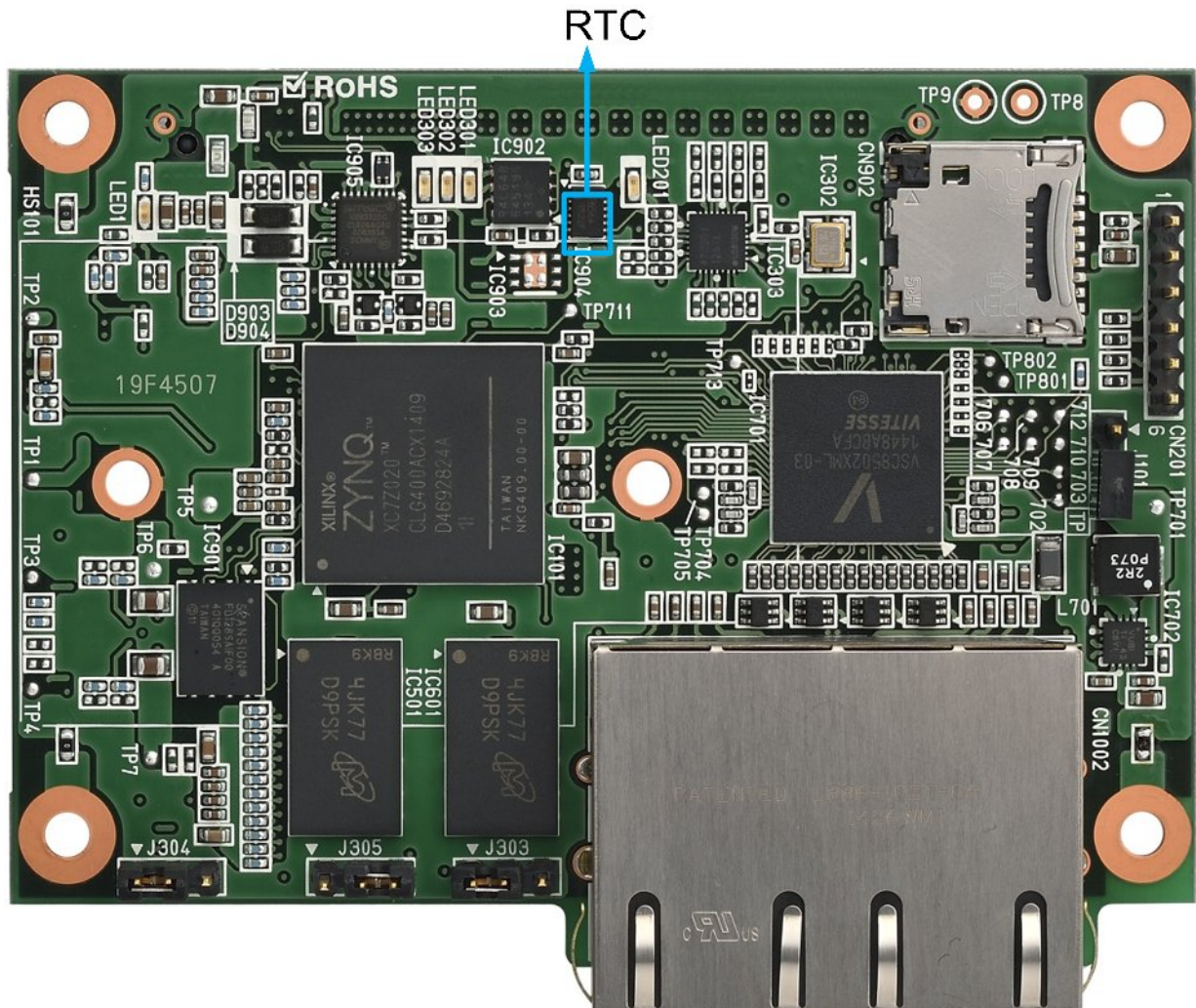


Figure 10-25 RTC

I2C slave addresses are as follows:

- ☐ I2C Write Address: 10100010 (0xA2)
- ☐ I2C Read Address: 10100011 (0xA3)

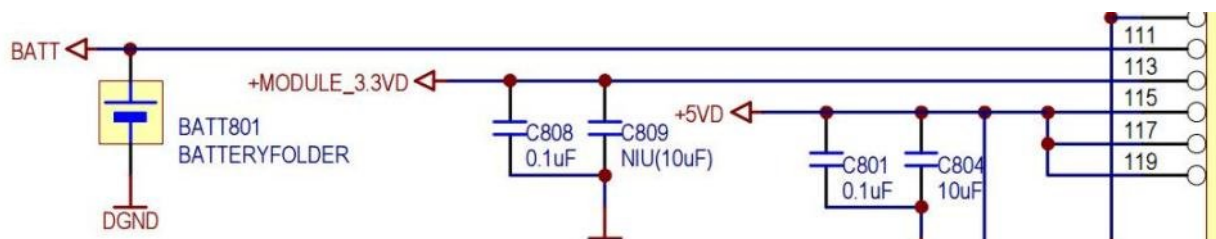
Table 10-12 shows the pin assignment between Zynq and RTC.

“Dir” shows the signal direction using Zynq as a yardstick.

**Table 10-12 Zynq - RTC pin assignment**

No.	Signal Name	DIR	Zynq Pin	Description
1	NC	-	-	No Connection
2	NC	-	-	No Connection
3	NC	-	-	No Connection
4	NC	-	-	No Connection
5	RTC_XINT	I	B5	RTC Interrupt, Active Low
6	DGND	-	-	Ground
7	PS_I2C_SDA	IO	C11	RTC Serial data address
8	PS_I2C_SCL	O	C10	RTC Serial clock, Fmax 400KHz
9	NC	-	-	No Connection
10	+3.3VD/BATT	-	-	RTC Power supply
11	DGND	-	-	Ground
12	NC	-	-	No Connection

Pin #10 (BATT) is connected to the B2B connector (CN901). The operation of a timer can be stably maintained by connecting a battery to the user board even when the Module is turned off.



**Figure 10-26 RTC battery connection**

[Operation of this function is confirmed with below.]

- CR2032



## 11. Boot Mode Setting (J303/J304)

The TB-7Z-IAE board can be booted either by QSPI Flash or microSD card. The boot mode can be selected using a short jumper.

**Important:**

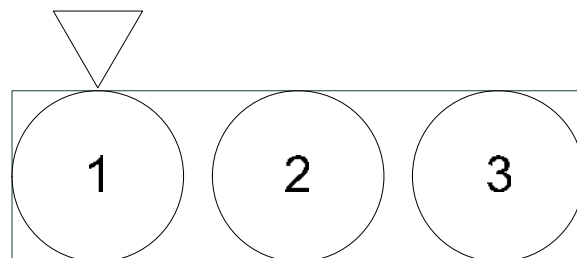
**Turn off the TB-7Z-IAE board and the user board before performing the mode selection.**

**Table 11-1 Boot mode setting**

Boot Device	J303	J304
JTAG	2-3(Low)	2-3(Low)
SD Card	1-2(High)	1-2(High)
QSPI	1-2(High)	2-3(Low)

**Figure 11-1** shows the boot mode setting pins.

The position of a triangular silk marking on the board indicates pin #1.



**Figure 11-1 Boot mode setting pins**

For more information about the boot mode, refer to XILINX's **UG585, Zynq-7000 Technical Reference Manual** (Chapter 6).

## 12. JTAG Mode Setting (J305)

The TB-7Z-IAE board allows the selection of the JTAG mode of Zynq.

When the JTAG connector (CN201) on the TB-7Z-IAE board is used, set the JTAG mode to Cascade Mode.

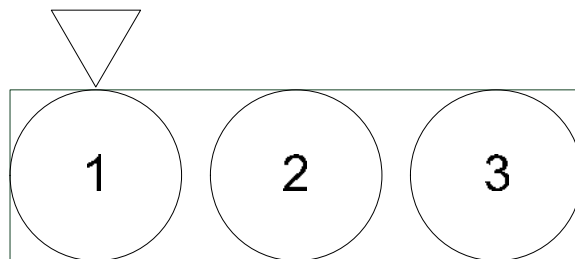
When ARM JTAG debugger is used via a B2B connector, set the JTAG mode to Independent Mode.

**Table 12-1 JTAG mode setting**

JTAG Mode	J305
Cascade	2-3(Low)
Independent	1-2(High)

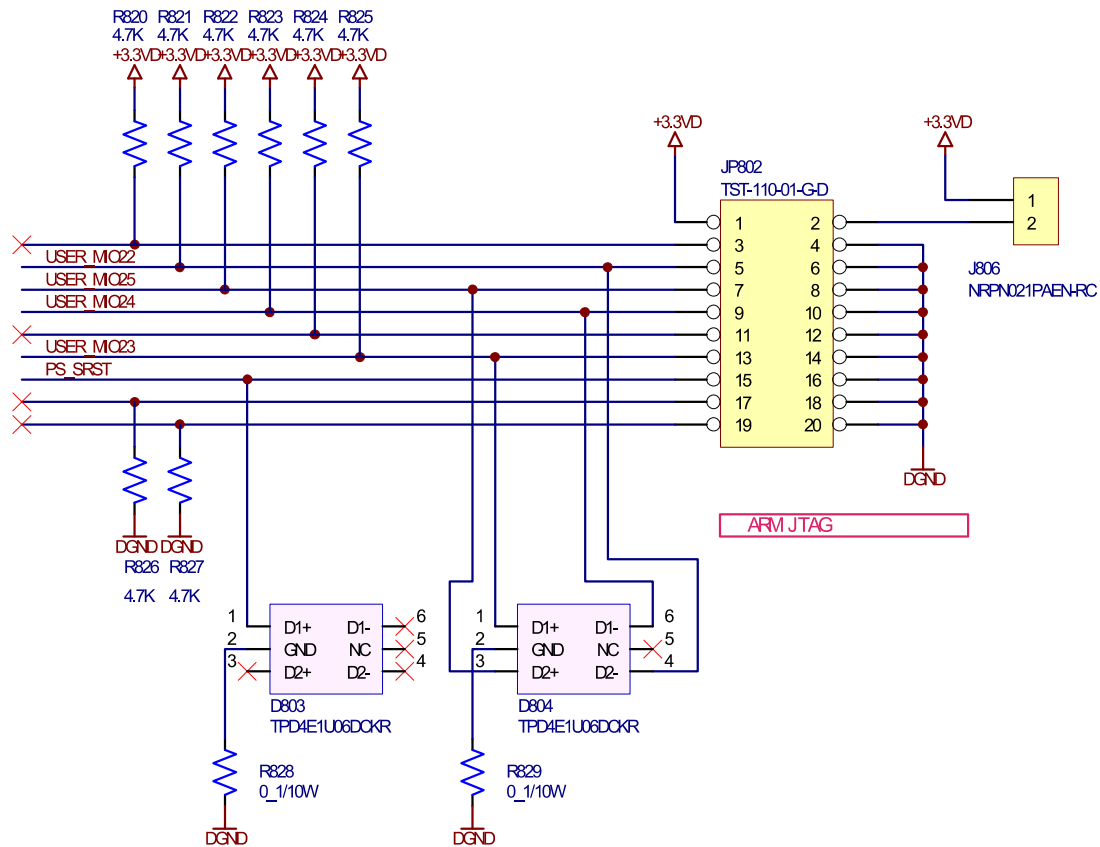
**Figure 12-1** shows the JTAG mode setting pins.

The position of a triangular silk marking on the board indicates pin #1.



**Figure 12-1 JTAG mode setting pins**

The circuit shown in **Figure 12-2** is an example of the ARM 20-pin type JTAG connector connected to the USER\_MIO22/23/24/25 pin of a B2B connector.



**Figure 12-2 ARM 20-pin type JTAG reference circuit**

For details about JTAG mode, refer to XILINX's **UG585, Zynq-7000 Technical Reference Manual** (Chapter 27).

### 13. Default Factory Setting

Figure 13-1 shows the default factory switch setting.

Check the switch setting at the area enclosed in a blue line.

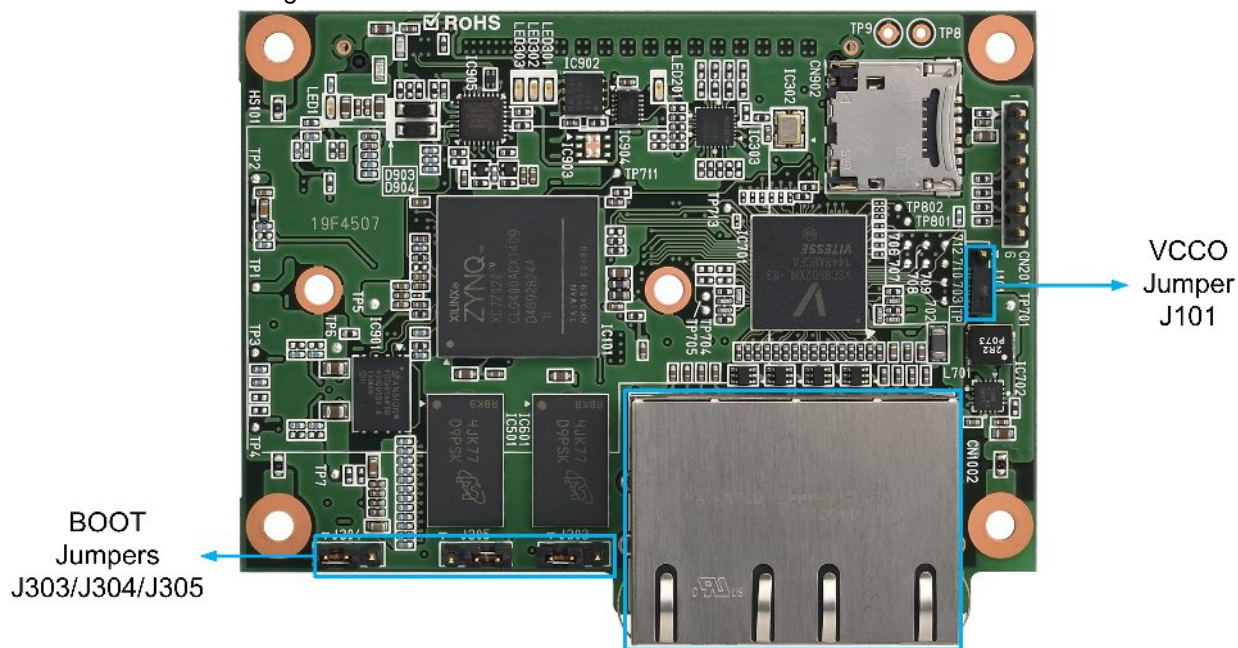


Figure 13-1 Component side

Table 13-1 Default setting

No.	Jumper	Setting	Note
1	J101	2-3	B2B USER_IOP/N: 2.5V
2	J303	1-2	Boot Mode: QSPI
3	J304	2-3	
4	J305	2-3	JTAG Mode: Cascade Mode





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